QUANTAR TECHNOLOGY

MODEL 2401B POSITION ANALYZER

INSTALLATION AND MAINTENANCE MANUAL

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STATEMENT OF LIMITED WARRANTY

Quantar Technology products are warranted against defects in material and workmanship for a period of one year from the date of shipment. During the warranty period, Quantar Technology will, at our option, repair, replace, or refund the purchase price of products which prove to be defective. For warranty service or repair, this product must be returned to Quantar Technology.

For products returned to Quantar Technology for warranty service, Buyer shall prepay shipping charges to Quantar Technology and Quantar Technology shall pay shipping charge to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, customs clearance charges and taxes for products returned to Quantar Technology from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

Special Notes regarding MCP's and products containing MCP's (microchannel-plate electron multipliers): Warranty does not cover damage to MCP's caused by warpage or cracking due to improper storage, shock, vibration, contamination or improper handling. Users are cautioned that MCP's are sensitive to water vapor absorption and may warp and crack if stored outside of clean vacuum systems for extended periods.

For sealed-tube detectors, warranty does not cover damage resulting from exposure to excessive input radiation levels, thermal shock, exposure to temperatures below 35° C, excessively rapid rates of change of temperature, mechanical shock or excessive high voltage applied to tube.

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SUCH EXCLUDED LOSSES SHALL INCLUDE, BUT ARE NOT LIMITED TO: COSTS OF REMOVAL AND INSTALLATION, LOSSES SUSTAINED AS THE RESULT OF INJURY TO ANY PERSON, OR DAMAGE TO PROPERTY.

SECTION 1. GENERAL DESCRIPTION

1.0   SCOPE OF THIS MANUAL

This Manual provides information regarding the installation, operation, adjustment and corrective maintenance of the Model 2401B Position Analyzer. For information concerning complete detector system set-up, checkout and operation, consult the 3300/2400 Series System Installation and Operation Manual and for detailed information on the 3300 Series MCP/RAE Sensors, consult the 3300 Series Installation and Maintenance Manual.

1.1   MODULES

The Model 2401B Position Analyzer is a high-speed, high-sensitivity, electronic charge-sensitive amplifier/shaper and pulse-position analyzer. It is designed for use as the readout electronics with a Quantar Technology UHV-compatible, Series 3300 Open-Face MCP/RAE Sensor for single-event, position-sensitive, multichannel imaging detection of relatively low-count-rate fluxes of electrons, positrons, neutral/negative/positive ions or low energy ionizing photons (UV or soft X-rays).

The Model 2401B is also used as part of the 2600 Series Single-Photon Imaging Detector Systems for position-sensitive optical photon detection; the Quantar Technology Model 3450A *Mepsicron*tm Imaging PMT and Model 2601 Photon Imaging Detector System provide single-photon, position-sensitive, multichannel imaging detection of optical photons from below 180 nm to above 900 nm, depending on the photocathode type selected, and can be used with scintillators for detection of hard X-rays, neutrons and gamma-rays.

Depending on the option ordered, the Model 2401B is supplied complete with the Model 24012 Charge-Sensitive Preamplifier/Shaper module, configured as either option EM (gain set to be compatible with standard-spatial-resolution 2 MCP sensors) or option EP (gain set to be compatible with high-spatial-resolution 5 MCP sensors). This preamp module is separately packaged so that it may be conveniently placed in close proximity to the detector.

1.1.0   MANUFACTURING HISTORY

The Model 2401A (A version) Position Computer was manufactured by Surface Science Laboratories Inc. and Surface Science Instruments Inc. from 1983 through 1988, and was manufactured by Quantar Technology Inc. from 1989 through October 1990. Several engineering changes were made during this period. The Model 2401B (B version) Position Analyzer was introduced by Quantar Technology Inc. beginning in October 1990 and includes several additional changes and improvements. Engineering design changes are described in Section 3.3, Engineering Design Changes, so this manual will be useful for older units as well as the latest versions, although full schematics are not included in this manual for all earlier versions.

1.2   SYSTEM CONFIGURATION

1.2.0   SYSTEM THEORY OF OPERATION

A typical vacuum-environment detector system consists of a Quantar Technology Series 3300 Open-Face MCP/RAE Sensor mounted in a suitable vacuum chamber, the Model 2401B Position Analyzer with the preamp, an auxiliary HV bias power supply and voltage divider network, an oscilloscope real-time monitor and a computer-based digital data collection system. The configuration for optical radiation detection is nearly identical with the exception that the sealed-type MCP/RAE Sensor does not require a vacuum environment for operation.

In operation, wafer-type electron multipliers (microchannel plates, MCP's) in the sensor amplify the incident particle flux so that each incoming particle provides a measurable pulse of charge on the resistive anode. This charge diffuses in the uniform resistive film and is divided among the four corner collection electrodes of the resistive anode in proportion to the spatial position of incidence. The four output charge signals are amplified and shaped by the preamp and then sent to the Position Analyzer. Using the sums and ratios of voltages from the preamps, the Position Analyzer performs a fast computation of the incident positions in the X and Y axes and provides analog pulse output voltages corresponding to each. Additionally, a blanking signal is generated for an oscilloscope real-time XY display. These outputs are typically connected to the X, Y and Z inputs of the scope which produces a real-time XY image of the incoming flux pattern.

1.2.1   PREAMPLIFIER OPTIONS

Depending on the option ordered, the Model 2401B is supplied complete with the Model 24012 Charge-Sensitive Preamplifier/Shaper module equipped with either option EM (gain set to be compatible with standard-spatial-resolution 2 MCP sensors) or option EP (gain set to be compatible with high-spatial-resolution 5 MCP sensors). In addition to a difference in gain, the charge amplifier compensation is also modified.

1.2.2   DIGITAL OUTPUT OPTIONS

Optional fast (130 Mhz clock rate) analog-to-digital converters provide a sampled digital representation (digital bin number) of the analog position voltage on each axis. The two digital words that are generated represent the position coordinate of the event on each axis.

The standard analog version or the version equipped with 8-bit A to D converters (option 008/EC) has a dead-time of about 4 μsec per event. The 9-bit (option 009/EE) and 10-bit (option 010/EJ) A to D converters require more resolving time, yielding a system dead-time of about 6 μs and 10 μsec respectively.

1.2.3   MCA INTERFACE OPTION

If the analog position signals are to be captured using an external ADC or pulse-height analyzer, such as an MCA (multichannel analyzer), it may be necessary to install the MCA Interface Option to the Model 2401 to translate the between-event analog signal voltage level to zero volts (rathr than the standard 2.5 volts) to enable proper operation of the external ADC or MCA, which often require the pulse leading edge to be only positive-going. See Section 3 of this Manual for a component locator and schematic of this option.

1.2.4   PULSE REJECTION

The system has several features which maximize position accuracy of data. Fast look-ahead circuitry (E channel) allows the processor to ignore signals which are too small to be properly processed, signals resulting from simultaneous or near-simultaneous events on the RAE, or events which have come too soon after the previous event to be properly computed (to a pulse-pair resolving time of approximately 400 nanoseconds). Thus for event input rates up to approximately twice the maximum output rate (1/dead-time) with a random time spacing between events, the processor will correctly compute the incoming event position. Beyond that rate, some attenuation must be provided ahead of the microchannel plates to achieve maximum accuracy.

1.2.5   DIGITAL MEMORIES AND SOFTWARE

Optional Histogramming Memory units provide digital data accumulation capability. These units receive the digital position address of each imaged event, and increment (histogram) a digital RAM memory counter corresponding to the appropriate image location. A host computer, under the control of software, reads out this data from the Histogramming Memory and displays the spectra or image data. These memory devices enable the acquisition of up to 20-bit wide spatial position addresses (up to 10 bits X and 10 bits Y, which address up to 1,048,576 memory bins or "channels"), provide hardware incrementing (histogramming) without direct host computer attention and free the host computer for other tasks during long accumulations. These memory units are typically physically mounted in the Model 2401B Position Analyzer and derive operating power from it.

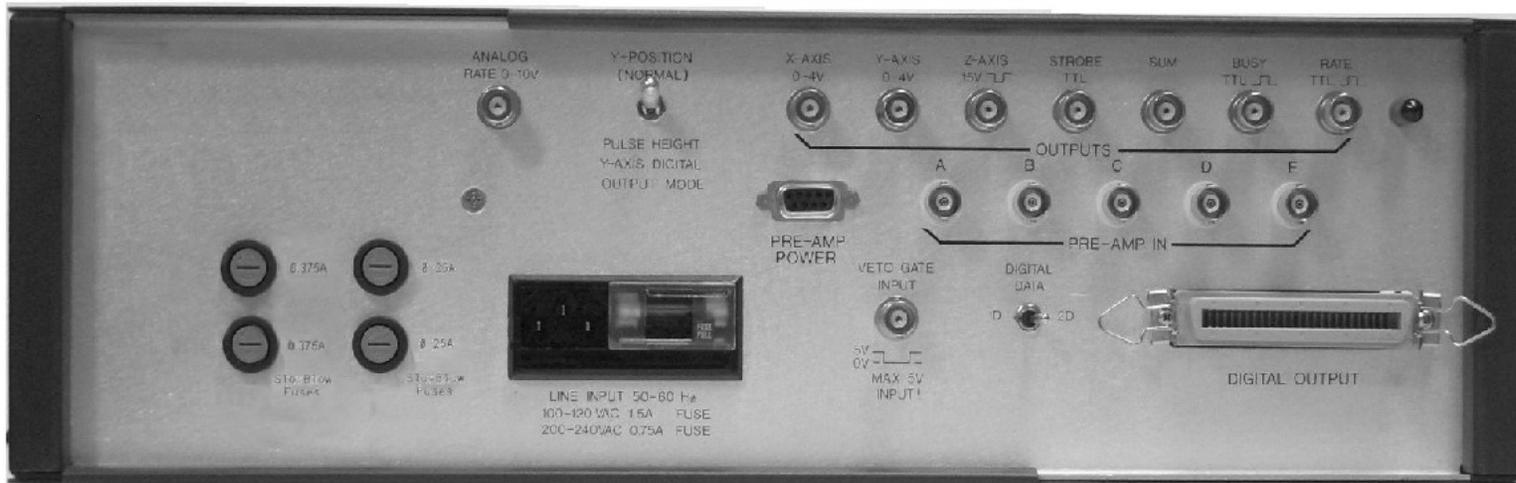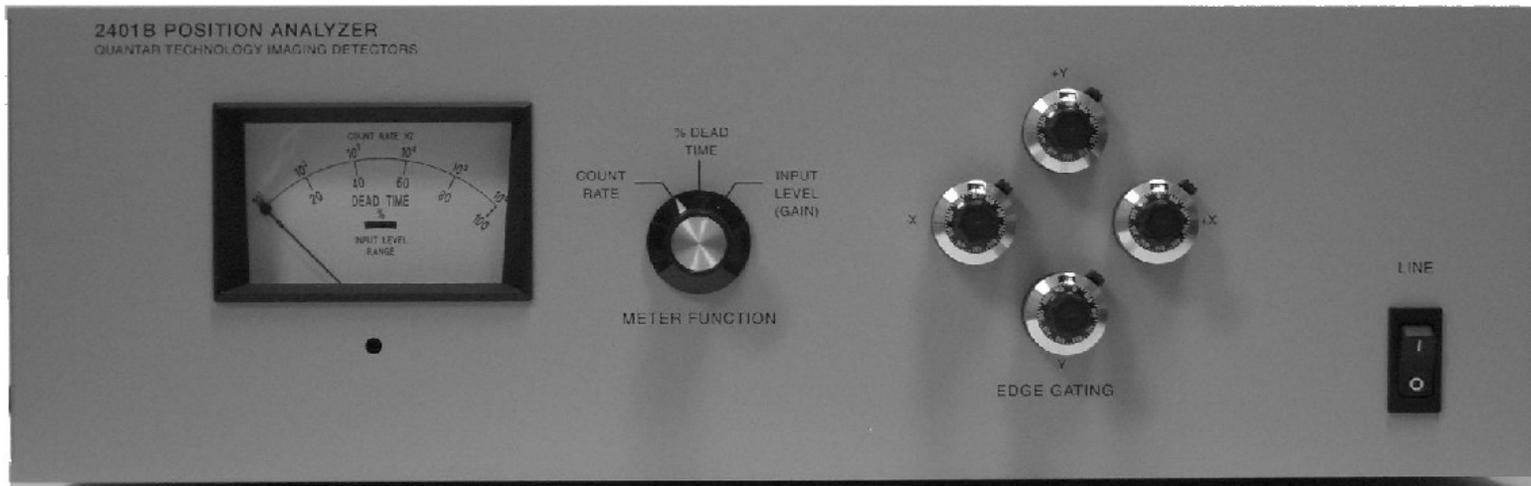Figure 1-1   Model 2401B Position Analyzer, Front and Rear Views

Figure 1-2   Preamp and Accessories Supplied

1.3 SPECIFICATIONS, Model 2401B Position Analyzer

SPATIAL RESOLUTION CAPABILITY:

Standard Unit (option EM): 100 resolvable elements (FWHM 1/100 of active diameter of sensor) with 5×10^6 electron gain in sensor (Models 3390, 3392 and 3394).

High Resolution (option EP): 400 resolvable elements (FWHM 1/400 of active diameter of sensor) with 5×10^7 electron gain in sensor (Models 3391 and 3395).

Spatial Linearity: Maximum of approximately 4% of full scale (active diameter) relative displacement of any point in the entire image. Output is monotonic over entire image. Includes fixed non-linearity of RAE.

DYNAMIC COUNTING RANGE:

Position Output
Dead-Time Per Event:

Analog only:	3.8 μsec
8-bit digitized output:	4 μsec
9-bit digitized output:	6 μsec
10-bit digitized output:	10 μsec

Maximum Output Rate
on X,Y Position Outputs:

Analog only:	110 KHz
8-bit digitized output:	100 KHz
9-bit digitized output:	75 KHz
10-bit digitized output:	60 KHz

Rate Output: Tracks true input event rate to approximately 100 KHz count rate (about 500 nsec paralyzable dead time per event). Indicates to above 1 MHz with increasing coincidence losses. Used for dead-time correction and pulse-pile-up rejection. Pulse-pile-up rejection time is approximately 400 nsec (closest spacing between events such that two events can be detected as being distinct events). Events with time spacing of less than 400 nsec are processed as single event, with spatial position as geometrical mean between events (an error), unless their combined amplitude exceeds the upper level discriminator, in which case they are vetoed from processing.

INPUTS: Imaging Channels A, B, C, D from preamp, Fast-Look-Ahead Channel E from preamp, Veto Gate Input.

OUTPUTS: Analog X Position, Analog Y Position, Z-axis Blanking, Analog Strobe, Sum, Busy, Rate, ±15 V power to preamp. Digital output versions include: Digital X position, Digital Y Position, Digital Strobe.

OTHER SPECIFICATIONS:

Recommended Load Impedances: X, Y, and SUM: 10K ohms minimum load
Z Axis: 500 ohms minimum load.

Digital Output Connector:	Single 50-pin, flat, D-ribbon, connector, 3M p/n 3565-1000 (mating connector - 3M p/n 3564-1001 or equivalent connector). Carries X, Y and STROBE digital signals. See Figures 2-1 and 2-2, Digital Output Connector Pinout.
Optional Histogramming Buffer Memory:	(Obsolete, no longer available) Models 2412A or 2415A Histogramming Buffer Memory units are compatible and may be installed in Model 2401 as a data system accessory. In this case, ADC output signals are routed directly to the memory input (using a ribbon-type Digital Memory Mapping Cable, DMMC) and do not appear on the rear panel connector. Instead, the digital lines from the memory to the host computer IO-interface appear on a single 50-pin rear panel connector. See Figure 2-1 for the main board connector output and the Manual for the 2412/2415A Histogramming Buffer Memory.

PHYSICAL CHARACTERISTICS:

Analyzer Electronics Module (19" Rack Unit):

Dimensions:	5 1/4"H (133mm) x 17"W (432mm) x 18"D (458mm), 22"D (560mm) with rear cables and front rack-mount handles.
Net Weight:	20 pounds (9.1 kg), with preamp and accessories.
Shipping Weight:	30 pounds (13.7 kg) approximate including preamp module and accessories.
Power Required:	100-120/220-240 VAC, 50-60 Hz, 75 watts maximum. Switchable power entry module fuses: 100-120 VAC, 1.5 A, AGC Normal (Fast) Blow; 220-240 VAC, 0.75 A, AGC Normal (FAST) Blow. Dual-output linear, modular supply fuses: +/-5V supply - 0.25A, AGC Slo-blow (qty - 2); +/-15V supply - 0.375A, AGC Slo-blow (qty - 2).

WARNING

The Model 2401B is equipped with a *switchable* AC power input module. To avoid serious damage, this module *must* be set to the appropriate LINE VOLTAGE *before* inserting the power cord. The operating voltage is set by the orientation of the small removable printed circuit insert card in the power module. To access this card, slide the plastic cover to the left and remove the PC card with thin pliers. Reinsert with the appropriate marking for

Preamp Module:

Dimensions:	7"L (178mm) x 5"W (127mm) x 2"H (51 mm)
Weight:	2 pounds (0.9 kg)
Power Required:	+15VDC @ 200 ma; -15VDC @ 200 ma: supplied by analyzer module (rack unit)
Accessories Included:	Multi-Cable Preamp-to-Analyzer Module Cable, 8 ft (2.7 m) length, 4 each RG-188 type coax cables (BNC one end, other unterminated) for preamp inputs, 18" (0.5 m) length, 2 each Rack-Mounting Adapter Brackets, 3 each BNC-to-BNC cables (X, Y and Z), Installation and Service Manual.

SECTION 2. INSTALLATION

2.0   MOUNTING OF ELECTRONICS MODULES

The main chassis of the Model 2401B Position Analyzer may be used either as a stand-alone unit or mounted in a standard 19-inch wide electronics rack using the rack mounting brackets supplied. Handles for convenience in lifting are mounted on the rack adapter brackets. When mounting in an electronics rack with other equipment, proper grounding procedures should be followed to avoid generation of noise and ground loop currents. For System Level Installation information, see the 3300/2400 System Manual.

The 24012 Preamplifier Module should be mounted as close to the MCP/RAE Sensor as possible to minimize lead capacitance at the input of the charge-sensitive circuits. It is recommended that the preamp be mounted to a common ground point on or close to the vacuum flange for the signal and HV vacuum feedthroughs. It may be mounted on a user-supplied metal bracket using two or more of the 4-40 size machine screws that can be seen on the bottom surface of the module case. It may be necessary to use slightly longer screws depending on the thickness of a mounting bracket. The bracket should then be mounted securely to the vacuum chamber. Even a few ohms resistance in this grounding path can result in ground loop noise voltages. It may be necessary to experiment with the optimum grounding procedure for a particular setup to minimize noise pickup (see SUM pulse diagnostic measurements, see CHECKING NOISE LEVEL, in 3300/2400 System Manual).

2.1   CONNECTING PREAMP TO POSITION ANALYZER

The preamp has 6 connections which go to the position analyzer, including 5 signal outputs and a power connector. Preamp outputs A through D correspond to position analyzer inputs A through D and carry amplified and shaped signals from the four corners of the RAE detector. Output E is a fast version (higher bandwidth) sum of the input signals to the preamp which is used by the position analyzer for look-ahead and pulse-pile-up rejection timing. Connect BNC connector A to A, B to B and so on. Signals A through D come from identical preamps and may be interchanged to correct for improper arrangement of the preamp input leads from the MCP/RAE sensor in the vacuum system (or PMT housing) or for purposes of troubleshooting (See 3300/2400 System Manual and Section 3 of this Manual). A 6-foot (2 m) cable is supplied for interconnecting these signals to the position analyzer. A longer cable up to 12 feet in length may be substituted without significant spatial-resolution degradation.

2.2   CONNECTING POSITION ANALYZER TO EXTERNAL DEVICES

The following sections discuss the function and characteristics of the rear panel outputs and switches on the Model 2401B Position Analyzer.

2.2.1 ANALOG X AND Y POSITION SIGNALS

These signals are the primary analog event position outputs from the system. They are intended to be connected to the X and Y axis of an oscilloscope producing a real-time monitor image of the incoming flux. They can also be connected to a user-supplied analog-to-digital converter or digitizing multi-channel-analyzer (MCA).

The amplitude voltage (of the valid flat top portion) of these pulsed position signals ranges from approximately 0.5 to 4.5 volts, and is linearly proportional to the coordinate position of the most recently processed event, starting from one edge of the active area diameter of sensor and ending at the other edge (along diameter on each axis). These signals should be read by external devices only during period when STROBE signal (see below) is valid. This assures these signals are properly settled. These analog position signals are present for the following times (which are slightly less than the total dead-time of the Model 2401 version being used): 3 μsec (analog only and 8-bit digitized output option), 5 μsec (9-bit option) and 8 μsec (10-bit option).

Note regarding use with external MCA's (multi-channel-analyzers): The inter-event (between event) resting point of these X and Y position signals is 2.5 volts. As a result, the leading edge of the X, Y (or both) position pulses of an event located to the left of and below (voltages below 2.5 volts on either axis) the image center will have a negative-going leading edge. This confuses some MCA-type pulse-height analyzers (especially those without an externally-triggered Sampled Voltage Analysis Mode) which require a positive-going leading edge on all input pulses to enable the proper sampling of the peak voltage. A special interface option is available for the Model 2401B, called the MCA Interface Option, for these situations and returns the inter-event voltage to 0 volts so the leading edge of the position pulse is always positive-going. Before Model 2401A serial number 7440, this option was supplied on a plug-in board. Starting with that serial number, the components are installed on a special section of the main board. Consult Quantar Technology for more information regarding this option.

2.2.2 Z AXIS

The X and Y outputs return to the center of the oscilloscope screen between event computations (2.5 volts on each axis). In order to eliminate the bright spot which would appear in the center of the display due to this dwell time, the Z-axis signal provides a properly timed 15 volt signal which blanks the crt screen, except at the time when the outputs represent a valid event computation, in which case a bright dot appears at the appropriate point on the screen. See following CAUTION before connecting this signal.

CAUTION

Do NOT connect or disconnect the Z-axis cable while either the oscilloscope or the 2401 is powered on. Due to the presence of appreciable voltages on the Z-axis of some oscilloscopes, the Z axis output circuit (U120) of the Model 2401 can be damaged if this is done. Always turn oscilloscope power and Model 2401 power OFF before connecting or disconnecting the Z-axis lead.

The timing of the Z axis signal is the same as the Strobe signal. The Z-axis signal changes from +15 V to 0 volts for approximately the following periods: 4 µsec (analog only and 8-bit digitized output options), 6 µsec (9-bit digitized output) and 10 µsec (10-bit digitized output). This Z-axis output is compatible with the Z-axis Intensity Blanking function on many but not all laboratory oscilloscopes (please consult the equipment's manual and/or specifications).

2.2.3 STROBE

The analog strobe signal is a TTL-level signal which normally goes to 5 volts for the time period during which the analog X, Y position signal outputs are stable and readable. It can be used to trigger external A-to-D conversion or other logic. Connect to digital frequency counter to monitor STROBE count rate to measure total number of fully-processed events per second. There is a single STROBE pulse generated for every valid, fully-processed event. Polarity is selected by a board-level STROBE jumper (see Control Logic Component Locator, Jumper is located next to IC U122; use 2 pins nearest edge of board for 0V to +5V leading edge; use 2 pins farthest from edge of board for +5V to 0V leading edge). Duration of the STROBE pulse is dependent on the digitized output options, similar in operation to the Z-axis. Note: RATE *is* monitored by the front-panel meter; STROBE rate is *not* monitored).

2.2.4 SUM

The sum signal is the arithmetic sum of the output signals from the four shaping preamps (channels A through D). It is a diagnostic signal for observing the total amplitude level of the pulses being deposited on the RAE from the MCP's, enabling the adjustment of the HV bias to the appropriate level to generate the proper MCP gain. The SUM signal can also enable observation of the random noise and transient pickup by the system which can be detrimental to performance.

2.2.5 BUSY

The busy signal is a, TTL-level signal which goes from 0 volts to a logical high when triggered by the RATE lower-level threshold comparator (about 150 mV) and indicates the BUSY one-shot circuit is in a timing sequence. The "busy" monostable produces a signal slightly longer than the pulse duration of the four shaper amplifiers (for a single detected event it has a 2.8 μsec duration) and is retriggerable. Any additional pulse arriving within the busy period of a previous pulse will retrigger the "busy" timeout and will result in a longer pulse duration. It is useful in observing the preamp-associated dead-time.

2.2.6 RATE

The RATE signal represents the total incoming rate of pulses which exceed the RATE threshold (150 mV on SUM signal). A separate RATE pulse is generated for each event that is time-separated by at least 400 nsec from a prior event. Pulse duration is 500 nsec and the leading edge moves from the TTL-low level to the TTL-high level. Pulses are further tested for level and timing before actual processing and some events included in RATE may be vetoed later from further processing. The RATE output is useful for determining actual (true) input rate as compared to output rate available at the strobe (imaged) output to determine the fraction of input pulses being processed, up to a RATE of approximately 250 KHz, at which point the dead time of the RATE signal itself (about 500 nse) will result in imperfect tracking of the true input count rate.

RATE includes events that will be later vetoed from Strobe due to edge-gating settings, failure to exceed the Strobe lower threshold (300 mV on SUM pulse), pulse-pile-up rejection (see dead-time discussion below) or pull-down of the external Veto Gate Input (2401B only). RATE will always equal or exceed STROBE. Ratio of STROBE to RATE enables calculation of fractional dead-time loss (1-ratio). The RATE output can be connected to a digital frequency counter for monitoring (adjust counter threshold carefully to avoid double counting). This signal is monitored by the front panel meter when the Meter Switch is in the Count Rate position.

2.2.7 VETO GATE INPUT (Model 2401B version only, beginning October 1990).

This input provides for external, time-based digital control of processing. Grounding of this rear-panel input interrupts both analog and digital output until it is released from ground. This capability is useful in applications where it is desirable to exclude processing of events to an external data system or memory except during specified periods which are synchronized to external experimental conditions (e.g low-rep-rate pulsed laser excitation of a sample). The precision (time-jitter) of this input in controlling the cut-on and cut-off of processing is approximately 300 nsec. This input is pulled up to the "normal status" by internal resistors when the input is removed from ground level. However, in no case should signals in excess of 5 volts be applied to this input.

If an event is NOT to be vetoed, the VETO GATE signal must be in high state no later than 20-30 nsec after the event occurs (when FAST RATE signal appears on U115b) and must continue to be in the high state up to approximately 800 nsec (peak time, PK-TH). If it is allowed to go low at any time in this interval, then the event will be vetoed from further processing. If event IS to be vetoed, the VETO GATE must be pulled LOW sometime before 500 nsec after the event occurs, and held low through about 800 nsec.

2.2.8 DIGITAL X AND Y POSITION SIGNALS

The digitized position output signals are TTL-level, positive-true signals and include the data lines (8, 9 or 10 lines), each with a separate ground connection, plus the Digital Strobe ("read-me" signal). The connector and cable pin designations are shown in Figures 2-1 and 2-2, Digital Output Connector diagrams.
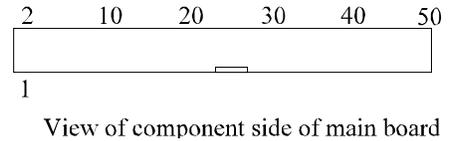
2.2.8.1 DIGITAL STROBE

1.5 μsec duration, negative true logic, TTL-level pulse that accompanies digitized position signals to latch data or trigger to be read by external data device (memory, computer, etc). Digital Strobe starts immediately at end of ADC conversion (later than the analog strobe), which depends on digital option. Not available on analog only versions. Goes from TTL-high level to TTL-low level on leading edge.

Figure 2-1   Digital Output Connector, Main Board, ADC Output

MAIN BOARD DIGITAL OUTPUT CONNECTOR

For units equipped with digital output options, digital TTL-level signals for both X and Y axes are available, together with the Digital Strobe and Rate signals. The connector pin assignments for the Digital Output Connector (the 50-pin header on the main board), are as follows:

ODD PIN #	FUNCTION
1	Y axis LSB, 2^0
3	Y axis
.	.
.	.
17	Y axis, used only for 9 and 10 bit options
19	Y axis, used only for 10 bit options
--	
21	X axis, LSB, 2^0
23	X axis
.	.
.	.
37	X axis, used only for 9 and 10 bit options
39	X axis, used only for 10 bit options
--	
41	STROBE (Digital)
43	RATE (Digital)
45	No connection (do not ground). After 2401B S/N 95467, with 1-D/2-D digitial switch circuit on main board, this pin is used for control of this function by rear panel manual switch.
47	No connection (do not ground)
49	No connection (do not ground)
EVEN PIN #	
26-50	Grounded (for each individual digital bit)

```
 2      10      20      30      40      50
┌──────────────────────────────────────┐
│                    ▭                   │
└──────────────────────────────────────┘
 1
```
View of component side of main board

For Model 2401 units equipped *with* one of Quantar Technology's optional Histogramming Buffer Memory modules (2412/2415 etc), the digitized output from the main board is connected to the input of the memory board. Consult the manual for the appropriate model memory board for pin assignments for the rear-panel 50 pin connector which differ from the above.

Verify desired configuration and part number before ordering.

Figure 2-2   Digital Output Connector, Rear Panel, ADC Output

REAR PANEL DIGITAL OUTPUT CONNECTOR (*WITHOUT* HISTOGRAMMING
MEMORY INSTALLED)

For units equipped with digital output options, digital TTL-level signals for both X and Y axes are available, together with the Digital Strobe and Rate signals. The connector pin assignments for the Digital Output Connector (the 50-pin 3M brand D ribbon connector on the rear panel) for units *without* a Histogramming Buffer Memory board installed only, are as follows:

View from rear panel

PIN #	FUNCTION
1	Y axis LSB, 2^0
2	Y axis
.	.
.	.
9	Y axis, used only for 9 and 10 bit options
10	Y axis, used only for 10 bit options
11	X axis, LSB, 2^0
12	X axis
.	.
.	.
19	X axis, used only for 9 and 10 bit options
20	X axis, used only for 10 bit options
21	STROBE (Digital)
22	RATE (Digital)
23	No connection (do not ground). After 2401B S/N 95467, with 1-D/2-D digitial switch circuit on main board, this pin is used for control of this function by rear panel manual switch.
24	No connection (do not ground)
25	No connection (do not ground)
26-50	Grounded (for each individual digital bit)
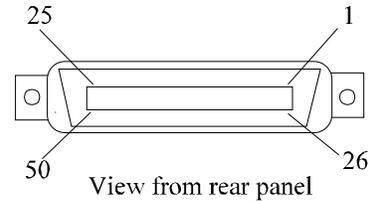
For Model 2401 units equipped *with* one of Quantar Technology's optional Histogramming Buffer Memory modules (2412/2415 etc), the rear panel 50-pin connector is used for the interface to a computer IO board from the memory board. The digitized output from the main board is connected to the input of the memory board. Consult the manual for the appropriate model memory board for pin assignments for the rear-panel 50 pin connector which differ from the above.

The current 3M Part Number for the 50-pin cable connector that mates to this rear panel connector is 3564-1001; other equivalent connectors from AMP or Amphenol should interface properly. Verify desired configuration and part number before ordering.

2.3   REAR-PANEL SWITCHES

2.3.1 Y-AXIS DIGITAL OUTPUT MODE SWITCH - PULSE HEIGHT MEASUREMENT

This switch, located on the rear panel, selects the input signal to be digitized by the optional Y Axis A-to-D converter. In the normal position, the converter digitizes the Y-Position signal. In the PHA position the input to the converter, together with a sample and hold to catch the pulse peak, is connected to the SUM pulse. This function therefore produces a digitized pulse height distribution which is useful for more precise evaluation of MCP gain (number of events on vertical axis and relative SUM pulse amplitude (gain) on the horizontal axis). Observation of this digitized Pulse Height Distribution requires a digital data collection system. The amplitude of the SUM pulse corresponding to a specific event indicates the size of the charge pulse that was deposited on the RAE by the MCP's in response to that event. It is, therefore, a direct indication of MCP electron gain. For an example of a typical Pulse Height Distribution, see the 3300/2400 System Installation and Operation Manual.

2.3.2 1-D/2-D DIGITAL MEMORY MAPPING CABLE MANUAL SWITCH (OPTIONAL)

This rear panel switch controls the mode of the optional Switchable Digital Memory Mapping Cable (Model 11006A, or 11005A Field Kit) linking the ADC output with the address input port of the Model 2412A, 2413A or 2415A Histogramming Buffer Memory. It enables switching between 1-dimensional (Y-axis only) and 2-dimensional (Y and X axis) operation without physically exchanging the Digital Memory Mapping Cable (flat multiconductor ribbon cable) which is normally required when changing between 1-D and 2-D data accumulation.

In 2401B units with SN 95467 and above (approx Dec 1995), this 1-D/2-D switching function is implemented on the main board. It is designed primarily to be controlled by Quantar Model 2251A MCA/MCA2D Software. It can be controlled by an optional rear-panel switch as well which is normally not installed. If the switch is installed, it must be left in the 2-D position in order for the software to be able to control the switching function. Consult the factory for details of installing this manual switch if desired.

2.4   DIGITAL DATA ACQUISITION SYSTEMS (models mentioned below are no longer available)

Acquisition of digital data can be handled using several different approaches.

Previously, the most convenient was to use a RAM-based, Histogramming Memory to collect data from the digital output ports of the Model 2401B Position Analyzer. The device collected counts with specific digital (spatial) addresses and auto-incremented the number of counts in the corresponding memory location by 1 count per event. The host computer, under control of appropriate software, then periodically reads out this memory, channel by channel. The Models 2412A and 2415A Histogramming Memory were configured for use with the Model 2420A/B Parallel IO Interface for PC/AT-compatible personal computers; Model 2251A 1-D Spectratrak and 2-D Imagetrak Software runs only under the DOS Operating System on the PC/AT host computer equipped with EGA (Enhanced Graphics Adapter) compatible video display.

To connect the PC/AT compatible data system, do the following:

1)   Install the Model 2420A/B Parallel IO Interface in an available slot in the PC.

2)   Install the Model 2415A Histogramming Memory and cables (see Model 2415A Installation and Operation Manual)

3)   Connect the Model 11001A GPIO (General Purpose IO) Cable from the Model 2420A/B IO Interface card to the Digital Output connector on the rear panel of the Model 2401B Position Analyzer.

4)   Load and properly configure the software (See Model 2251A Software User Guide).

See the Model 2251A Software User Guide and the Model 2415A Histogramming Memory/Model 2420B Parallel IO Interface Manuals for additional information. Other data systems may also be available including data systems for time-resolved spectroscopy and imaging. Contact Quantar Technology for details.

SECTION 3. MAINTENANCE

3.0   ELECTRONIC ADJUSTMENTS

The Model 2401B Position Analyzer as supplied requires no internal adjustments. However, with aging or component replacement, it may be necessary to make minor adjustments. Refer to Figure 3-1, Adjustment Locator Diagram. An electron source is useful when making the following adjustments (a UV source will typically produce a low, unsaturated pulse height (gain) distribution which will make PHD measurements more difficult).

Y Full Scale: Set such that the maximum voltage at extreme +Y edge of circular MCP image is 4.5 volts. The -Y edge will then be about 0.5 volts.

+Y Gate: Set Full CW.

-Y Gate: Set Full CCW.

X Full Scale: Set in the same manner as Y Full Scale.

+X Gate: Set Full CW

-X Gate: Set Full CCW.

Fast Threshold: Set such that input signals >150 mv on the sum output produce an output pulse at the rate output.

Threshold: Set such that input signals >300 mv on sum output produce a pulse on the strobe output.

Gain Monitor: This adjustment sets the threshold only for the circuit that drives the input lever meter function. It is set such that the output on pin 2 of U120 goes high for pulses > 1.75 volts at the sum output.

Log Zero: This calibrates the Rate Function on the meter by setting the crossover point of the log signal. Connect a counter to the RATE output on the rear panel. Apply a constant rate input signal to the detector in the range of 1000-10000 counts per second. Adjust the Log Zero Trimpot such that the meter agrees with the counter.

Analog-to-Digital Converter (ADC) Adjustments: (Digital Output options only)

Zero and Span
Adjustments: The controls adjust the analog position voltage that corresponds to digital channel 0 and the maximum channel number (256, 512, or 1024 depending on option) and thus the "overlay" of the analog and digital images. These adjustments interact somewhat so several adjustment iterations typically are necessary. The exact adjustment procedure depends somewhat on the nature of the signal available. For example, if a sharp image feature can be moved around the image field to the edges, it can be used as a marker to adjust the zero and full scale levels. Alternatively, a shadow mask can be placed over the detector with small apertures at the respective extremes of the image field or a flood-source background can be used to identify the edges of the detector in each axis.

The analog output signals are unaffected by the ADC adjustments so they can monitor the position of the input test pattern during these adjustments. The digital image must be monitored by a data system while these adjustments are made. Generally, it is desirable to leave several (4-5) non-accumulating (dead) digital channels at each edge to prevent pile-up of counts in the first and last digital channels.

PHA Offset: After the zero and span adjustments are made, the PHA offset should be adjusted to give a zero slope intercept for pulse heights. A precision charge pulser connected directly to a pre-amp is useful for this adjustment.

1. First, set the ADC zero and span full-scale of Y axis properly. This ADC adjustment will affect PHA setting later, so ADC adjustment should be made first.

2. Connect a suitable pulse generator (preferably a tail pulser to emulate output from MCP/RAE sensor, each pulse consisting of about 10^{-12} coulombs of charge in a 200-300 nsec period, with a gradually decreasing pulse tail) to preamp inputs. Adjust relative inputs so imaged spot is at ZERO position on Y axis.

3. Connect a scope to "Test Point 1" (TP 1) on Y-axis ADC, monitoring ADC ramp (see ADC Schematic, Model 2401B Manual). Just before ramp starts downward, there is a flat area on waveform for several hundred nanoseconds. Note position of this section of waveform on scope vertical axis.

4. Flip Y-Axis Digital Mode switch to PHA position. Now you should see same portion of waveform near zero level. Adjust PHA OFFSET until this waveform portion is at same vertical position as noted in Step 3.

Ratio Circuit
Offset Null: This adjustment should only be necessary if replacing ratio circuit components. Disconnect inputs to the four pre-amplifiers A, B, C and D and short resistor R100 with a clip lead. Connect a high impedance digital voltmeter to pin 8 of Q201 and adjust R229 to obtain a reading of 0 ±0.1 mV. Repeat this procedure for Q212/R424, Q301/R329, Q312/R342.

Selection of
Strobe Signal
Polarity: To change polarity of strobe signal, move the jumper so as to short the center and left (for negative-going leading edge strobe) or center and right (for positive strobe) pins (See Figure 3-1 for jumper location).

Figure 3-1   Model 2401B Adjustment Locator Diagram
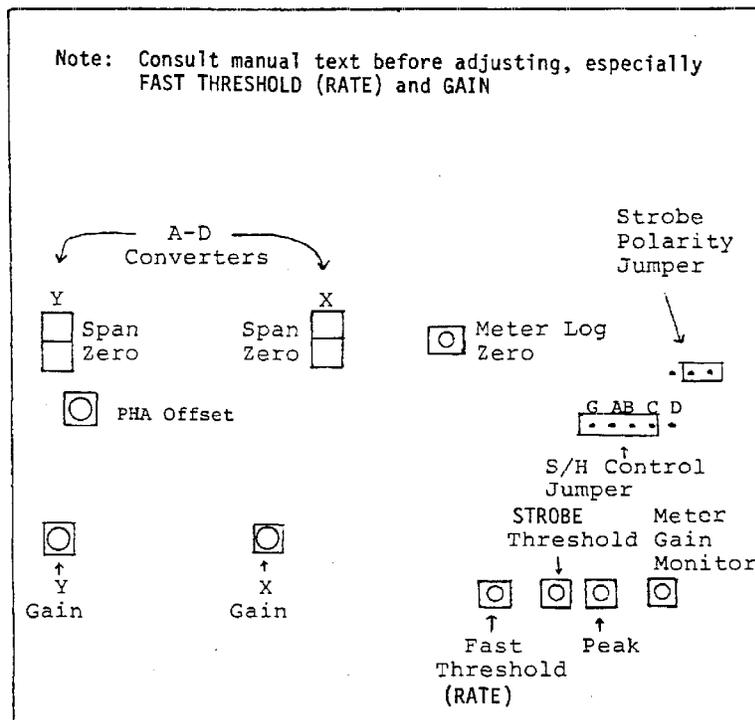
3.1   PRINCIPLES OF CIRCUIT OPERATION

3.1.0   GENERAL SYSTEM DESCRIPTION

The complete detector system includes an open-face or sealed-type MCP/RAE Sensor, charge-sensitive/shaper amplifiers, HV bias supplies, position analysis electronics and optionally, a computer-based data collection system. The resistive anode encoder is placed behind two or more microchannel plate electron multipliers having a total of approximately 5×10^6 to 5×10^7 gain, so each incident electron produces a detectable charge pulse on the anode. The operational function of each system component is described briefly in this section and is followed by a technical description of each circuit section sufficient to enable troubleshooting and problem correction by personnel familiar with these types of electronic circuits. Full schematics and component locators are included in Section 3.2

Figure 3-2   System Functional Diagram
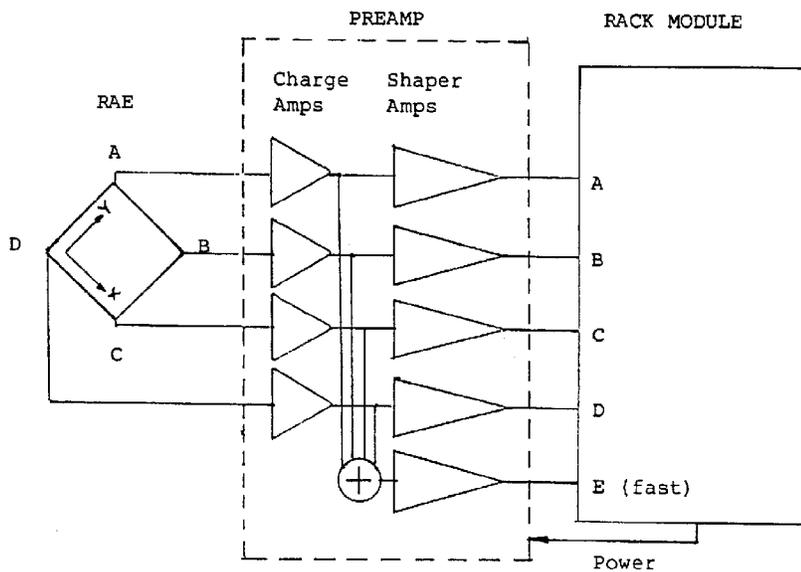
1)   The resistive anode encoder (RAE) is a diffusive RC transmission line which produces charge division between 4 output contacts (A,B,C,D) proportional to the position of the center of gravity of the charge pulse.

2)   The charge-sensitive/shaper amplifiers convert the low-level charge pulses into higher level shaped bipolar pulses suitable for input to the position analyzer electronics. The amplifier shaping network has been specifically matched to the resistive anode for optimum signal-to-noise ratio, short pulse duration and low baseline shift (for maximum counting rate capability).

3)   The position analyzer electronics generate an analog voltage output proportional to pulse position coordinates according to these formulas.

RATIO FORMULAS

$$X = \frac{B+C}{A+B+C+D}$$
$$Y = \frac{A+B}{A+B+C+D}$$

The position analyzer logic selects acceptable pulse processing and enables a sample/hold gate which stores selected events for a short time. Once an event pulse has been analyzed and its position signals are available at the X and Y outputs, a strobe pulse is generated.

4) Optional analog-to-digital converters (ADC) sample the analog XY position signals and generates an equivalent digital word representing spatial position as X and Y bin numbers.

Figure 3-3   Charge Amplifier/Shaper Block Diagram and Timing
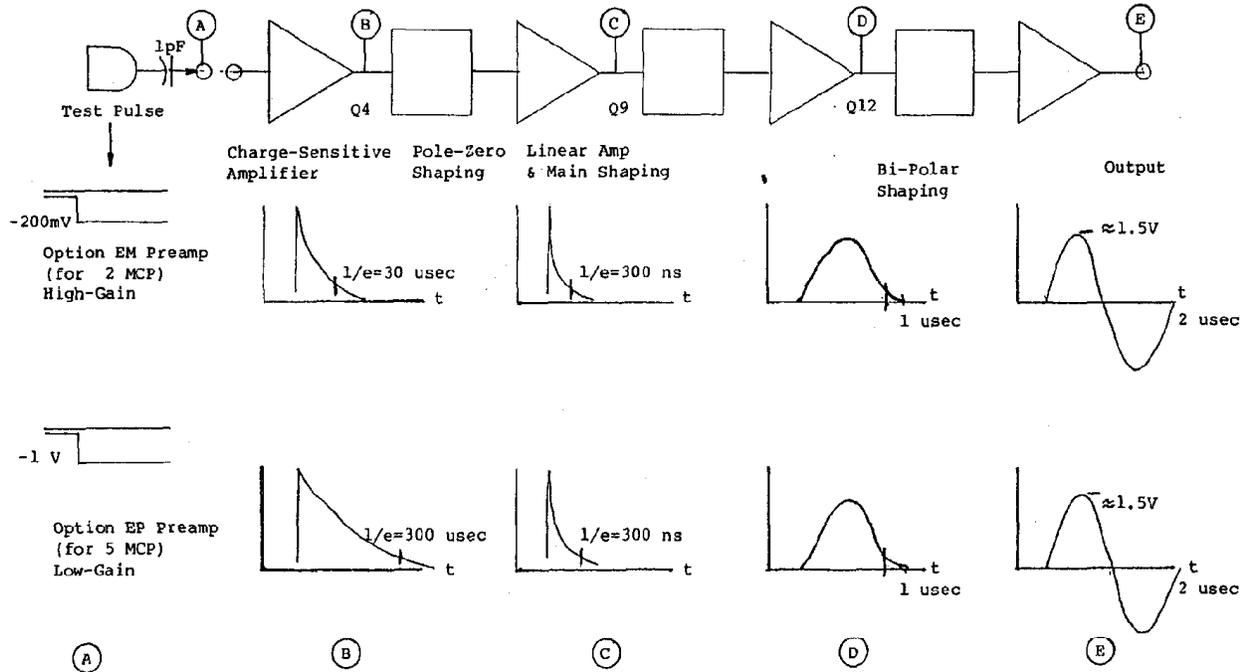
3.1.1   CHARGE-SENSITIVE/SHAPER AMPLIFIERS, SA-02 (imaging) and SA-02F (fast)

The Model 24012 Preamp module contains five amplifier circuits: Four SA-02 shaping amplifiers and one SA-02F fast shaper. Each SA-02 shaper amplifier consists of a charge sensitive preamplifier, a pole-zero canceling network and a series of gain and pulse shaping stages as illustrated in Figure 3-3. The overall gain for the option EM (for 2 MCP sensors) is 7.8 volts/pico-coulomb of charge input (early units had gain of 3.8 volt/pico-coulomb) with a shaping time (time-to-peak) of about 1.0 microsecond. The gain of option EP preamps (for 5 MCP sensors) is approximately 1.6 volts/pico-coulomb (measured at preamp output). The shaping network is an improvement over standard RC or semi-gaussian shaping and produces highly symmetric, fast settling shaped pulses optimized for low noise and high count rate.

The circuit schematics are shown in detail in Figure 3-12. Transistors Q1 - Q4 and associated components form the charge sensitive preamp. The feedback network contains R2 and C3 (plus C2 in the high-resolution EP option) which determine the charge gain and preamp time constant.

The pole-zero canceling network and gain trim are formed by R16-R18 and C3. Capacitor C3 is a gain trimmer which has been factory adjusted to match each of the 4 imaging channel amplifiers in the preamp to each other.

The first voltage amplifier contains Q7 - Q10. Gain is established by R19 and R20. This stage also provides the low impedance drive for the main shaping network, consisting of L1, L2, C11 - C15, R24 and R25. Transistors Q11 and Q12 form the second voltage amplifier. This stage also isolates the main shaping network from the bipolar differentiation network, L3, C16 and R33.

The output amplifier, consisting of Q13 - Q16 and associated components provides a low impedance output.

Fast Shaping Amplifier

Amplifier E is an SA-02F fast shaping amplifier whose input is the sum of the input signals to the charge sensitive pre-amps of amplifiers A, B, C and D. It includes an input voltage amplifier comprised of Q5 and Q6 with a gain of 6.5. The remaining stages are similar to the SA-02 but provide a shaping time that is ten times shorter. The output from this amplifier/shaper provides "advance information" to the Control Logic circuits regarding event amplitude and event timing for event rejection, regardless of spatial position of incidence.

Figure 3-4   Simplified Block Diagram, Position Analyzer
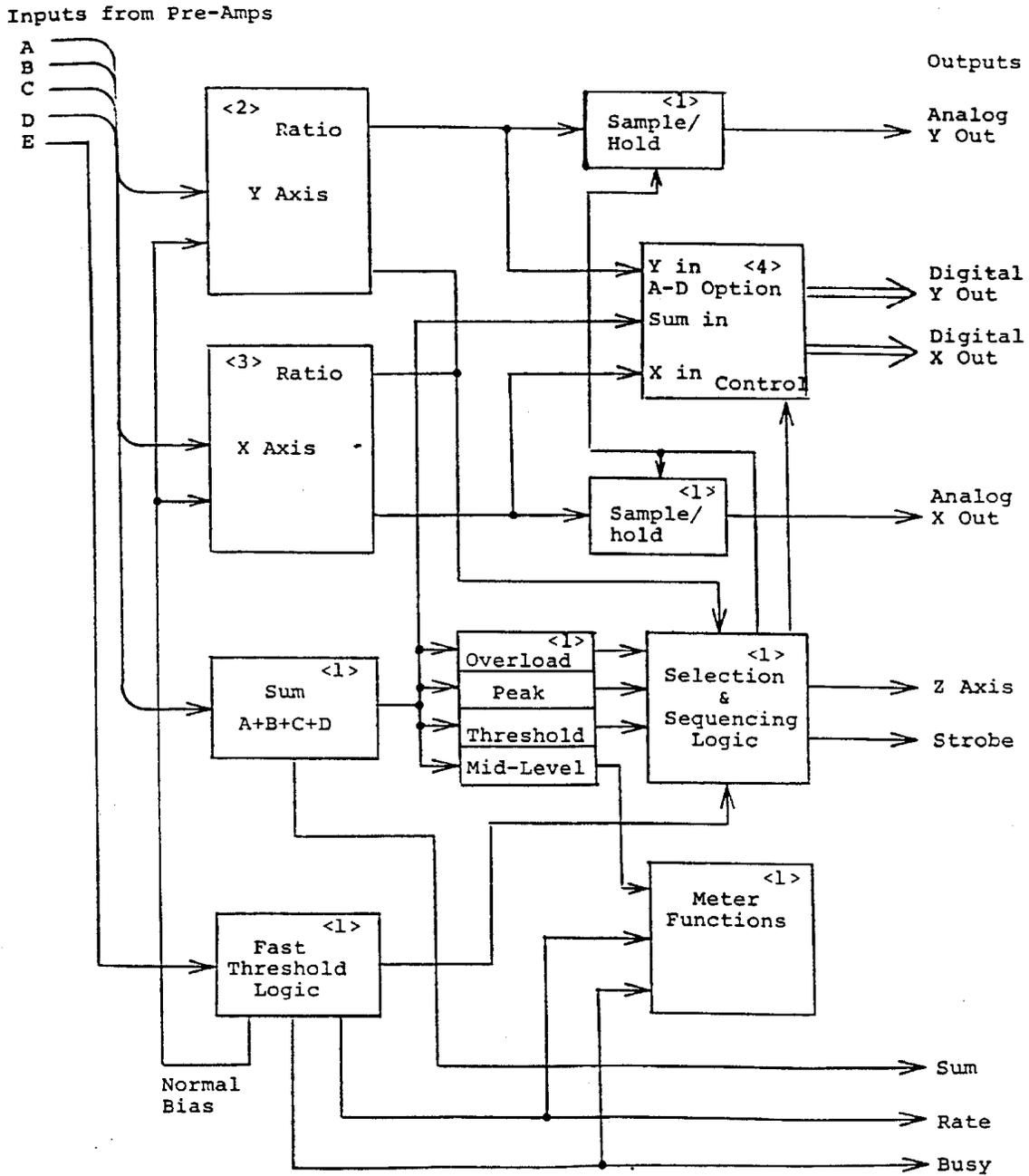
3.1.2   PULSE POSITION ANALYZER

A simplified block diagram of the position analysis circuits is provided in Figure 3-4. Bipolar input pulses from shaper amplifiers A, B, C and D are routed through ratio circuits which generate the analog position signals. The fast pre-amp signal "E" together with the sum signal A + B + C + D are used by the control logic to select acceptable events and initiate a sequence of logic control signals. Digitization of position signals or pulse height by the optional ADC is also governed by the control logic.

In this text and on the Schematics and Component Locator diagrams, each major circuit function is identified by a < > symbol. Schematics and Component Locator diagrams are in Section 3.2.

3.1.2.0   <1> CONTROL LOGIC

The main functions of the control circuitry are to select incoming pulses that are suitable for analysis and generate the necessary control signals for the ratio and ADC circuits. An acceptable input pulse must be a single pulse which (1) starts from a zero baseline and (2) has a peak amplitude lying between the threshold and overload discriminator levels. Time-overlapping pulses are also detected and rejected.

a.   Threshold Logic

Pulses from the fast "E" pre-amp that exceed the threshold of comparator U105 trigger the "busy," "normal bias" and "rate" monostables. The "busy" monostable produces a signal slightly longer than the pulse duration of the four shaper amplifiers and is retriggerable. Any additional pulse arriving within the busy period of a previous pulse will retrigger the "busy" timeout and also trip U115b which sets the "veto" line. The "normal bias" is turned off during the position analysis (to avoid indeterminate states in the ratio circuits due to the temporary absence of the denominator term) but returns slightly before the end of "busy" to guarantee that the ratio circuits have time to re-settle before another pulse is accepted. The "rate" pulse is intentionally much shorter than "busy" and is produced by a non-retriggerable monostable and thus represents the true count rate whereas the "busy" signal will become paralyzed at high rates.

b.   Sum Amplifiers

Amplifier U102 sums the four input pulses with an overall gain of one-half. Its output drives the peak detector and level discriminator comparators and two "sum" signal buffers U101 and U103. The SUM signal is available on the rear panel for test purposes and the "Clamped Sum" is used by the ADC for the pulse height analysis mode.

c.   Level Discriminators and Peak Detector

Level discriminators U106b and U107a,b establish threshold "TH," midscale "MID" and overload "OL" levels for the sum signal. The peak detector U106a compares a prompt and delayed sum pulse and switches near the peak of the pulse. The peak position is adjusted by R121. The coincidence of "PK" and "TH" initiates the control sequence but "OL" can cancel the sequence at U114a. The midscale "MID" signal is used by the "Input Level (Gain)" meter circuit.

d.   Selection and Sequence Logic

(See Figures 3-9 and Figure 3-10 for typical event cycles). The rising edge of PK-TH clocks U115a which starts a control sequence. U115a remains set until the busy signal ends so any subsequent U115a change will be ignored until "busy" time out. The output of U115a starts the U109a "short busy" cycle and also clocks U111b which samples the state of the "MID" level discriminator. The trailing edge of "short busy" resets the sequence logic at the end of event and occurs slightly before the end of the main "busy" signal thereby assuring that the sequence logic will be completely settled before another event can begin. The leading edge of "short busy" clocks the state of the "overload" discriminator into U114a. If the sum pulse exceeds the overload level, U114a will remain unset and the sequence will abort. If no overload is present, U114a becomes set and enables "PHA hold" if the PHA mode is selected, and also clocks U114b which samples the "veto" signal. A veto can be caused either by a pulse time overlap, detected by U115b, or by an edge veto signal from one of the ratio circuits, or by an external input (ground) at the rear-panel VETO GATE input (Model 2401B only). If no veto exists, U114b is set and the event is accepted.

Once an event is accepted, various control signals are generated. The "S/H" signal opens the analog switches U112, leaving the position signals stored on the storage capacitors (C128, C129). In addition, the "start convert" and "S/H" signals are sent to the ADC circuit iIf the ADC option is installed, and the U116a "ADC timeout" is started.. The Z Axis and Load Register signals go low, and the Analog Strobe is generated.

There are two options that affect the control sequence at this point. If the system has either the internal ADC option or is used with an external ADC without a sample/hold circuit, the "ADC timeout" triggers on the leading edge of the U114b signal, and its duration is set slightly longer than the maximum ADC cycle time (which depends on 2401B digital output option). The end of "ADC timeout" enables the U109b "reset" signal to clear the sequence logic for a new event.

If the system is used with an external ADC that has its own sample/hold such as a multichannel analyzer, then the 2401 can provide single-event pipeline storage. This option improves the total throughput rate if the external ADC cycle is longer than 4 usec (analog only or 8-bit digital output option) or 6 usec (9-bit) or 10 usec (10-bit). For this configuration the "ADC timeout" is started by the falling edge of U114b and its duration is set slightly longer than the maximum ADC cycle time. If a second event occurs during the "ADC timeout" period, the analog outputs retain the new data until the end of the timeout period, when the Analog Strobe goes high. The external sample/hold of the MCA should read data on the trailing edge of the analog strobe. These two options for ADC timing are selected by installing the appropriate jumper connections at the input of U116a (see note on Control Logic schematic <1>).

e.   Meter Functions

Three meter functions provide useful diagnostic information. These functions are selected by the front panel switch and include logarithmic count rate, dead-time and input level (sensor gain).

•   Log Count Rate Meter

The rate signal from U121b is a 0.5 μs wide logic pulse which turns on analog gate U112. The average current flowing through U112 is proportional to count rate. This current flows into the logarithmic current-to-voltage converter circuit consisting of U119, Q101 and associated components. This circuit makes use of the logarithmic current-to-voltage characteristic of the emitter-base junction of Q101 to produce an output voltage proportional to the log of the count rate. The nominal gain of this circuit is 2 volts per decade and the "zero level" can be adjusted with R155 (see Figure 3-1, Adjustment Locator Diagram).

•   Dead-Time Percent Meter

The "busy" signal also turns on a gate of U112 and causes a current proportional to the percent dead-time to flow through the meter. The slow meter response smooths these fast current pulses to give an average reading. *This reading is only approximate.*

•   Input-Level (Gain) Meter

The gain level meter function gives an indication of detector pulse gain. Each input event that trips U115a causes U111b to sample the state of the "mid" discriminator. The output of U111b is buffered and drives a charge pump consisting of C123, D103 and R168 that supplies current to the meter. The output signal is proportional to the fraction of pulses that exceed the "mid" level, so a midscale meter indication means the median of the detector pulse height distribution is equal to the "mid" discriminator level. For typical pulse height distributions the "mid" level is set to trip when the "sum" level exceed 2 volts.

Figure 3-5   Y-Axis Ratio Amplifier, Simplified Schematic
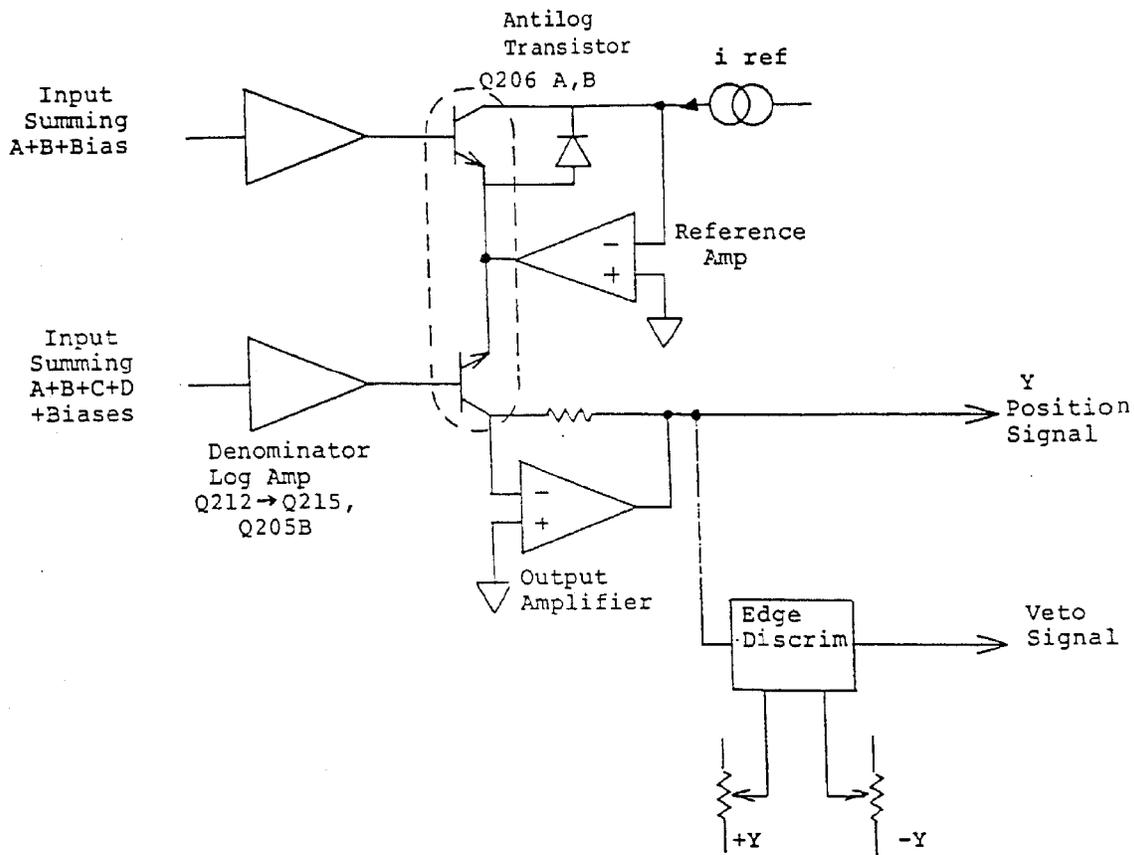
3.1.2.1   <2> <3> X, Y AXIS RATIO CIRCUITS

Operation of the X and Y axis ratio circuits is identical so a detailed description is given only for the Y axis circuit. The Y-axis ratio amplifier, shown in Figure 3-5 in simplified form, provides an analog output signal proportional to the ratio of the numerator and denominator input signals. This ratio is generated by a one quadrant log-antilog divider which exploits the logarithmic current-voltage characteristic of semiconductor junctions. Due to difference in circuit layout on the PC board, the Y axis may generally exhibit slightly better spatial resolution (less position jitter) versus the X-axis and therefore should be the chosen axis if data from only one axis is being used. If necessary, the X and Y coordinate axes can be exchanged by reversing the A and C input leads to the preamp from the MCP/RAE sensor.

a.   Input Summing

Input signals consist of various combinations of amplified anode inputs A, B, C and D as well as a bias signal. The "normal bias" signal is supplied at all times when a pulse is not present and is switched off by the control logic threshold circuit. The purpose of the normal bias is to maintain maximum response speed of the log amps by keeping the log feedback loop active at all times. Input signals are resistively summed at the log amp virtual ground input. The Y numerator signal is (A+B + Normal Bias) and the denominator is (A+B+C+D + Normal Bias). The only change made for the X axis circuit is that "C" replaces "A" at the numerator input. Numerator signal input resistors actually consist of two resistors in parallel to also match the input capacitance of numerator and denominator input networks.

b.   Numerator and Denominator Log Amps

Transistors Q201-Q204 and associated components comprise a transconductance amplifier which receives non-linear feedback via Q205a to produce an output voltage proportional to the logarithm of the numerator input current. Resistor R229 is an offset null adjustment, diode D201 prevents reverse breakdown of Q205A when negative input signals are applied, and R209/C200 and R222/C229 provide frequency compensation. In addition to the logarithmic voltage relation resulting from its semiconductor properties, the log transistor emitter-base voltage includes a contribution from the ohmic bulk resistance which can cause errors of several percent at maximum signal levels. This error term is canceled by feeding a small fraction of the input voltage to the base of Q205 via R200, R201 and R208.

The denominator log amp consists of Q212-Q215 plus Q205B and is essentially identical to the numerator circuit. Dual transistors Q205 is a monolithic matched pair which ensures good thermal matching of the two log amps. The bulk resistance compensation to the base of Q205B also includes a contribution from the position output signal which cancels the junction resistance error of the antilog transistors Q206.

c.   Antilog Transistor and Reference Amplifiers

The log subtraction and antilog functions are performed by the antilog transistors Q206a,b in conjunction with the reference amplifier comprised of Q205-Q210. The base of Q206a is connected to the numerator log amp and is at a voltage (-log N). Similarly, Q206b's base voltage is -log D, where N and D are the respective numerator and denominator input signals. If V_e is the emitter voltage of Q206a and b, the collector currents are expressed:

$$\log I_a = (-\log N) - V_e$$

and

$$\log I_b = (-\log D) - V_e$$

or

$$I_a - I_b = (N/D)$$

The reference amplifier adjusts V_e to produce a constant collector current $I_a = I_{REF}$ to Q206a. This reference current is set by R253 plus R254.

d.   Output Amplifiers

The antilog output current from Q206b is converted to a voltage by U201. The resulting voltage output of U201 is the desired ratio signal:

$$V_{out} = N/D = (R252)/(R252 + R254) \times 10.0 \text{ volts}$$

This is an idealized equation which ignores the various error terms that have been minimized by using matched transistors and bulk resistance compensation. Transistor Q211 serves to clamp the output signal between -0.7V by forward conduction and about +6V by zener breakdown.

e.   Edge Discriminators

A veto signal is produced by comparators U202 whenever the position signal falls outside the limits set by potentiometer R256 or R257.

f.   X-Axis Circuits

The X and Y axis circuits are nearly identical. Component numbers correspond by changing the first digit from 2 to 3, i.e. R3xx corresponds to R2xx.

3.1.2.2   <4> ADC OPTIONS

This option includes a pair (one for each axis) of Wilkinson-type A/D converters (ADC's) and the necessary control logic to interface with the standard 2401B control circuit. The Wilkinson converter technique uses a linear ramp voltage-to-time converter to switch a gated counter and exhibits excellent differential linearity (uniform bin widths). The ADC option can be ordered with 8-bit (256 channels), 9-bit (512 channels) or 10-bit (1024 channels) resolution (this is the number of "data points" distributed across the 0.5V to 4.5V range of the analog position signal in each axis) by choice of component values and jumper connections. Conversion times for the ADC conversion only are close to 2, 4 and 8 usec for the respective configurations. Normally the two ADC's are connected to the X and Y axes. A pulse height analysis mode can be activated by switching the Y-axis ADC input to the SUM signal in place of the Y-axis position signal for temporary diagnostic purposes.

A digital conversion begins when an event is accepted by the position electronics and the analog position signals for each axis are stored on a sample/hold capacitor. A counter begins counting pulses from a 130 MHz oscillator and simultaneously a current source starts a linear discharge of the sample/hold capacitor. When the capacitor voltage crosses a comparator "zero" level, the counter is stopped and its contents are loaded to an output latch. The outputs are latched until the next event is output.

The detailed sequence of events during a conversion is summarized as follows:

1)   The S/H signal from control logic <1> turns off analog gates.

2)   After a delay of about 100 ns (50 ns in earlier units) to compensate for analog gate switching, the control logic sends a "start convert" signal.

3)   The discharge current source is enabled on the first edge of the 130 MHz converter clock following "start convert."

4)   After a delay of three more clock periods, the counter is enabled by removing its reset signal. This delay is introduced to compensate for current source turn-on delay and for propagation delay of the zero crossing comparator.

5)   The counter continues counting clock pulses until the zero crossing comparator switches.

6)   The "load output" signal transfers data to output latches at the end of a conversion cycle.

7)   The end of "start convert" turns off the current source and resets the counter.

Input signals from either X and Y position circuits <2>, <3> or the sum amplifier <1> are switched through analog gates of U402 by the sample/hold signal from the control logic <1>. The Y axis channel can be converted to a pulse height analysis mode by the PHA select switch. Apart from the PHA mode, the two ADC's are identical. The detailed circuit description is given for the Y axis only.

a.   PHA Mode

The PHA Mode switch disables the Y axis analog gates and switches control to the "PHA hold" signal. The analog signal from the sum amplifier is clamped and level shifted to match the 0.5 to 4.5 volt range of the analog position signals. The "PHA offset" can be adjusted by R401 to align the zero level of the PHA with the position zero.

b.   Current Source

The capacitor discharge current source is a current mirror configuration comprised of dual transistor Q401a,b and amplifier U405. The current source is adjusted by setting the reference current through resistors R407 and R413, and is disabled by steering current through Q403. The current is enabled by the clock synchronized "start convert" signal coming from U410.

c.   Zero Comparator

The signal stored on capacitor C405 is buffered by U404 and sent to the "zero comparator" U409. The comparator input is clamped at a maximum of +1.3V by diodes D401 and D402, and R406 adjusts the comparator "zero level."

The comparator output signal passes through U410 for clock synchronization and thence to the clock enable of U416.

d.   Counters and Latches

Emitter coupled logic circuits U413-U419 form the counter strings of the two converters. Counter overflow is prevented by including one counter stage more than is used for the output data. The extra stage is connected to the preset of all previous stages, thereby locking the count to all "1's" in the event of overflow. A jumper connection is provided to select an 8-, 9- or 10-bit maximum count. Counter outputs are translated to TTL logic levels in U420-U424 and are latched at the end conversion in U425-U429. The output signals are all TTL levels.

e.   ADC Component Values for 8-, 9- and 10-Bit Operation

The 2401B ADC can be operated with optional full-scale ranges of 8, 9 or 10 bits. Although configured at the factory for a specified digital resolution, the component values corresponding to each option are given in Figure 3-16, Component Values for ADC Options, and jumper positions are shown on the ADC Schematic Diagram and ADC Component Locator, refer to Section 3.2.

3.1.3   WAVEFORMS

In addition to various oscilloscope photos shown, indicating the relationship between various waveforms in certain circuits, the Event Timing Diagrams are illustrated in Figures 3-9 and 3-10.

Figure 3-6   Upper, RATE pulse; Lower, SUM pulse: Vert=2 V/cm, Horiz=500 nS/cm
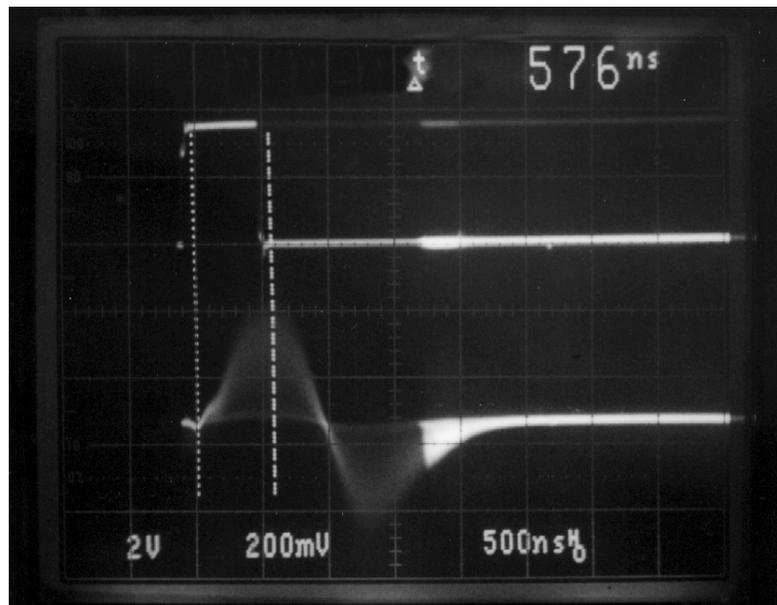
Figure 3-7   Upper, RATE pulse; Lower, STROBE pulse (10 bit ADC): Vert=2 V/cm, Horiz=2 μsec/cm.
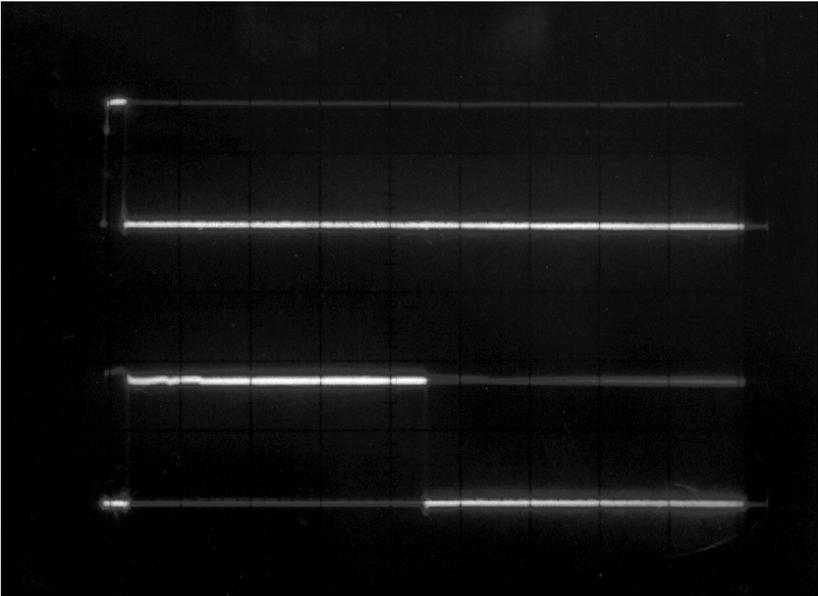
Figure 3-8   Upper trace, STROBE (10 bit, negative polarity); Lower, XY Position; Vert=2 V/cm, Horiz=2 μsec/cm
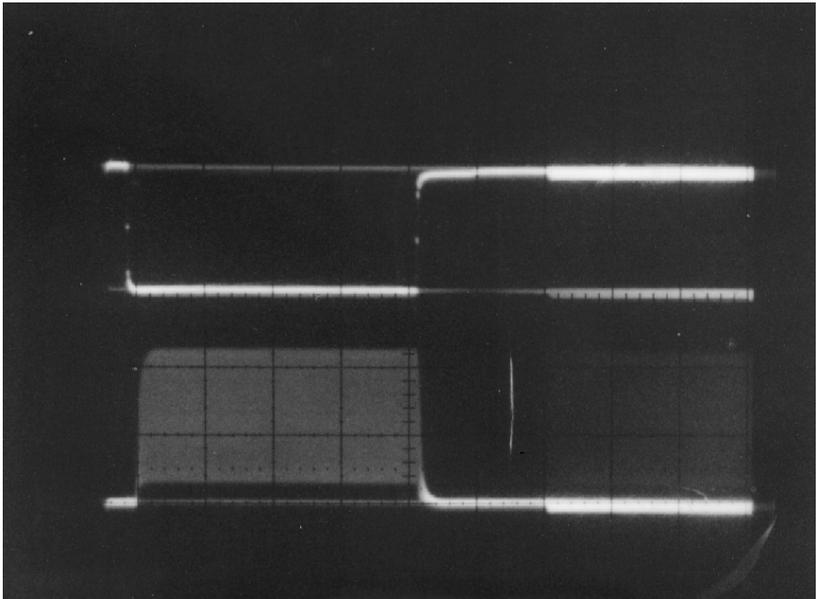
Figure 3-9 Event Timing Diagram, Analog Only and 8-bit Digital Output Option

E PREAMP
OUTPUT

RATE
OUTPUT, TTL

PEAK-THRESHOLD
COINCIDENCE

SUM OUTPUT
(ANALOG)

Average 1.75 V

X, Y POSITION
OUTPUT
(ANALOG)

4.5V

0.5V

STROBE OUTPUT

BUSY
OUTPUT, TTL

ELAPSED TIME
μSEC

0   1   2   3   4   5   6   7   8   9   10 μSEC

ADC
START CONVERT

ADC RAMP (TP 1
OR TP 2)

0 V

DIGITAL DATA
STROBE

COUNTER RUN

COUNTER ENABLE
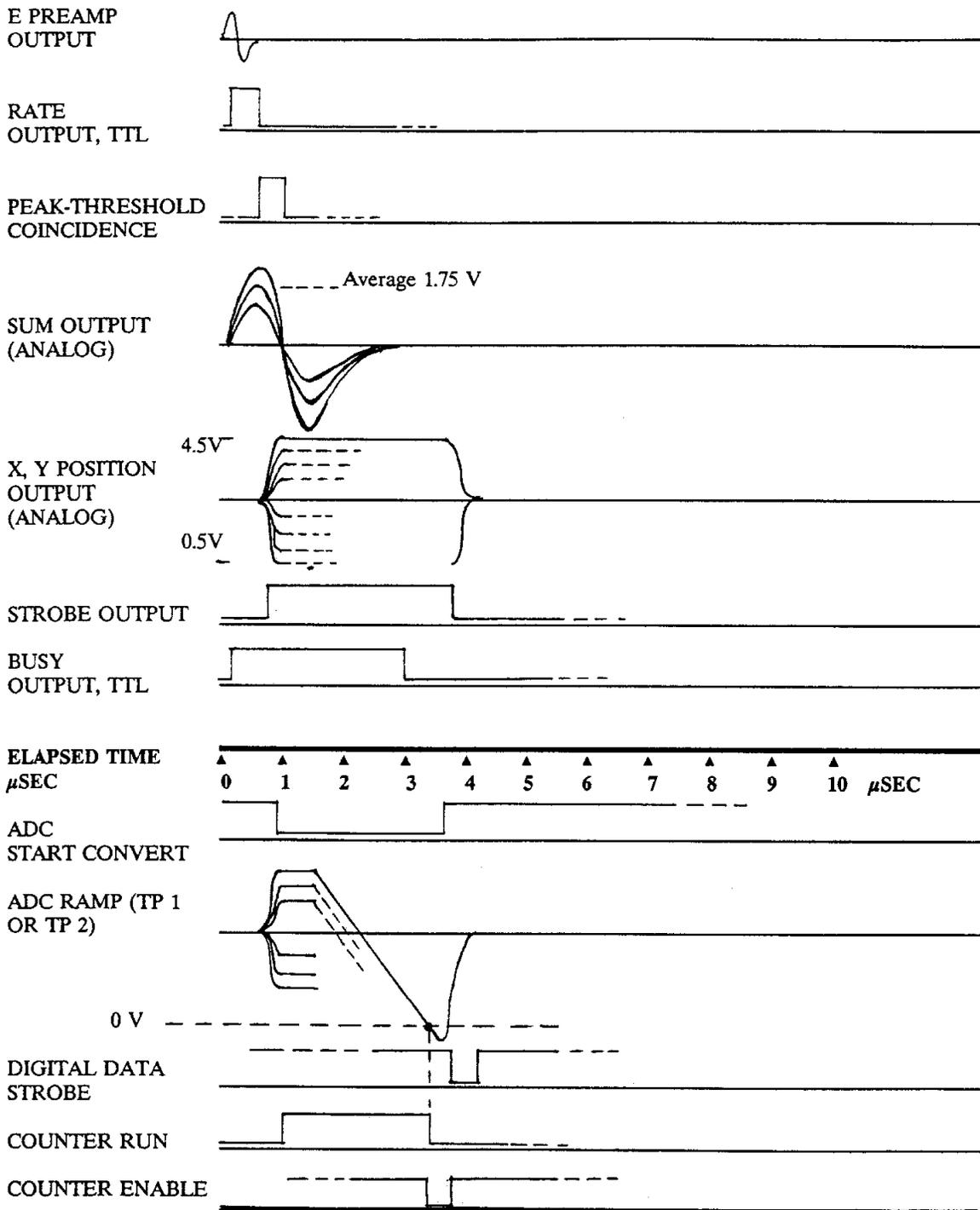
Figure 3-10   Event Timing Diagram, 10-bit Digital Output Option

E PREAMP
OUTPUT

RATE
OUTPUT, TTL

PEAK-THRESHOLD
COINCIDENCE

SUM OUTPUT
(ANALOG)

Average 1.75 V

X, Y POSITION
OUTPUT
(ANALOG)

4.5V

0.5V

STROBE OUTPUT

BUSY
OUTPUT, TTL

ELAPSED TIME
μSEC

0   1   2   3   4   5   6   7   8   9   10 μSEC

ADC
START CONVERT

ADC RAMP (TP 1
OR TP 2)

0 V

DIGITAL DATA
STROBE

COUNTER RUN

COUNTER ENABLE
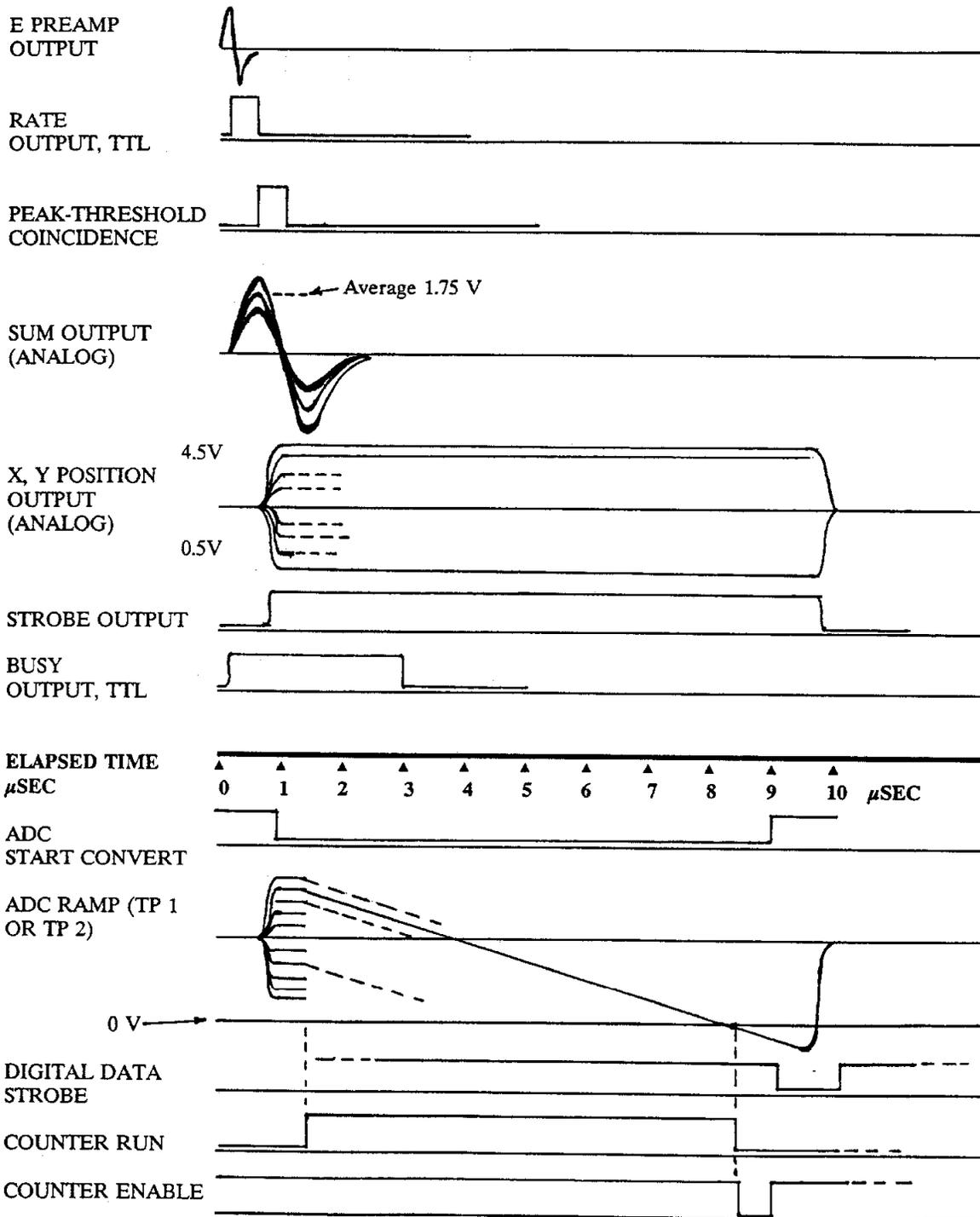
3.2   SCHEMATIC CIRCUIT DIAGRAMS AND COMPONENT LOCATIONS

3.2.0   SERIAL NUMBER

The following schematic circuit diagrams and component locators apply to Model 2401 Position Analyzer boards with serial numbers of 95467 and above (starting with units manufactured approximately December 1995). For schematics for earlier units, contact Quantar Technology.

Figure 3-11   Main Board, 2401 (S/N 7440 and above). Earlier versions had cutout at rear right corner (for MCA)
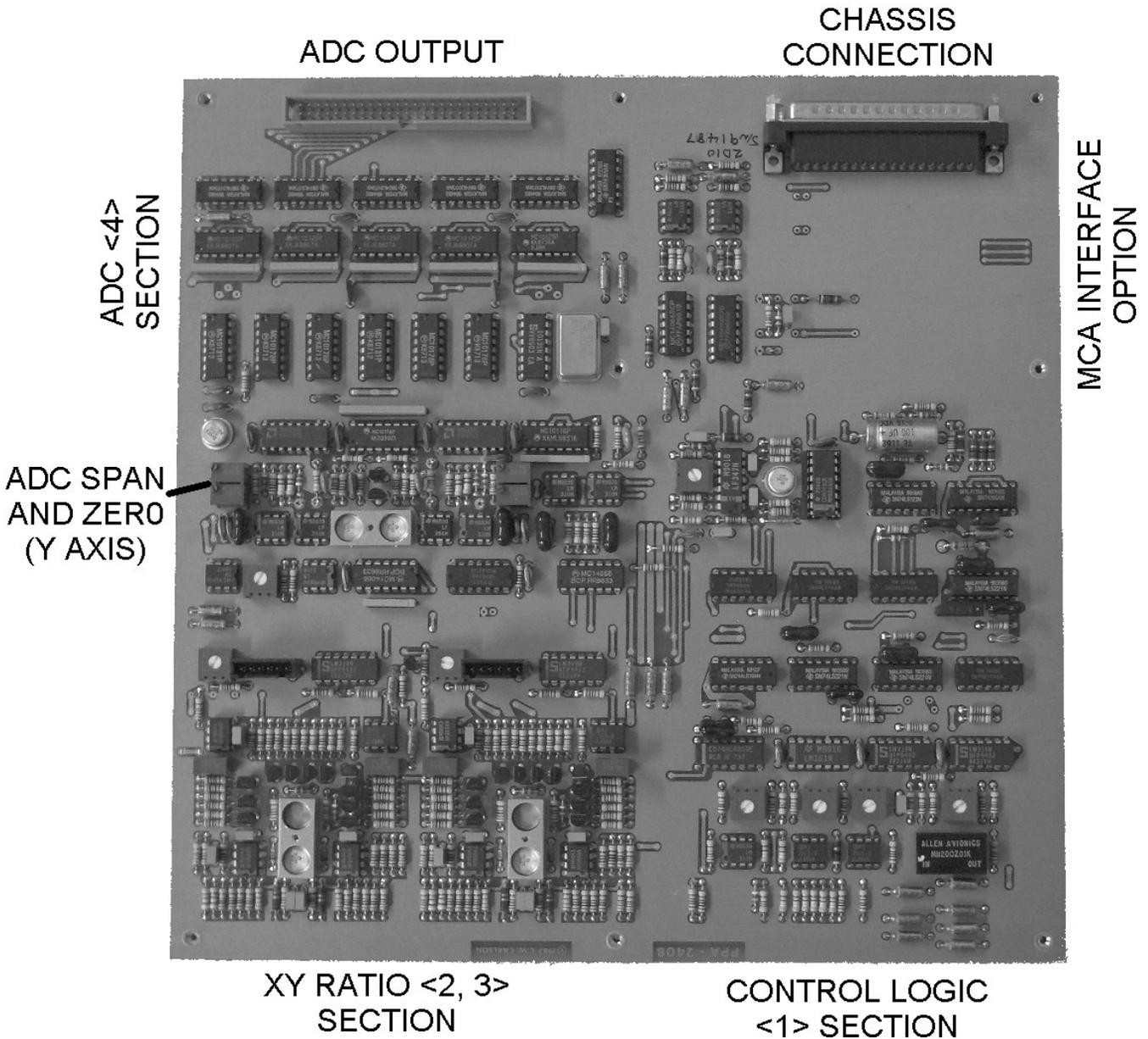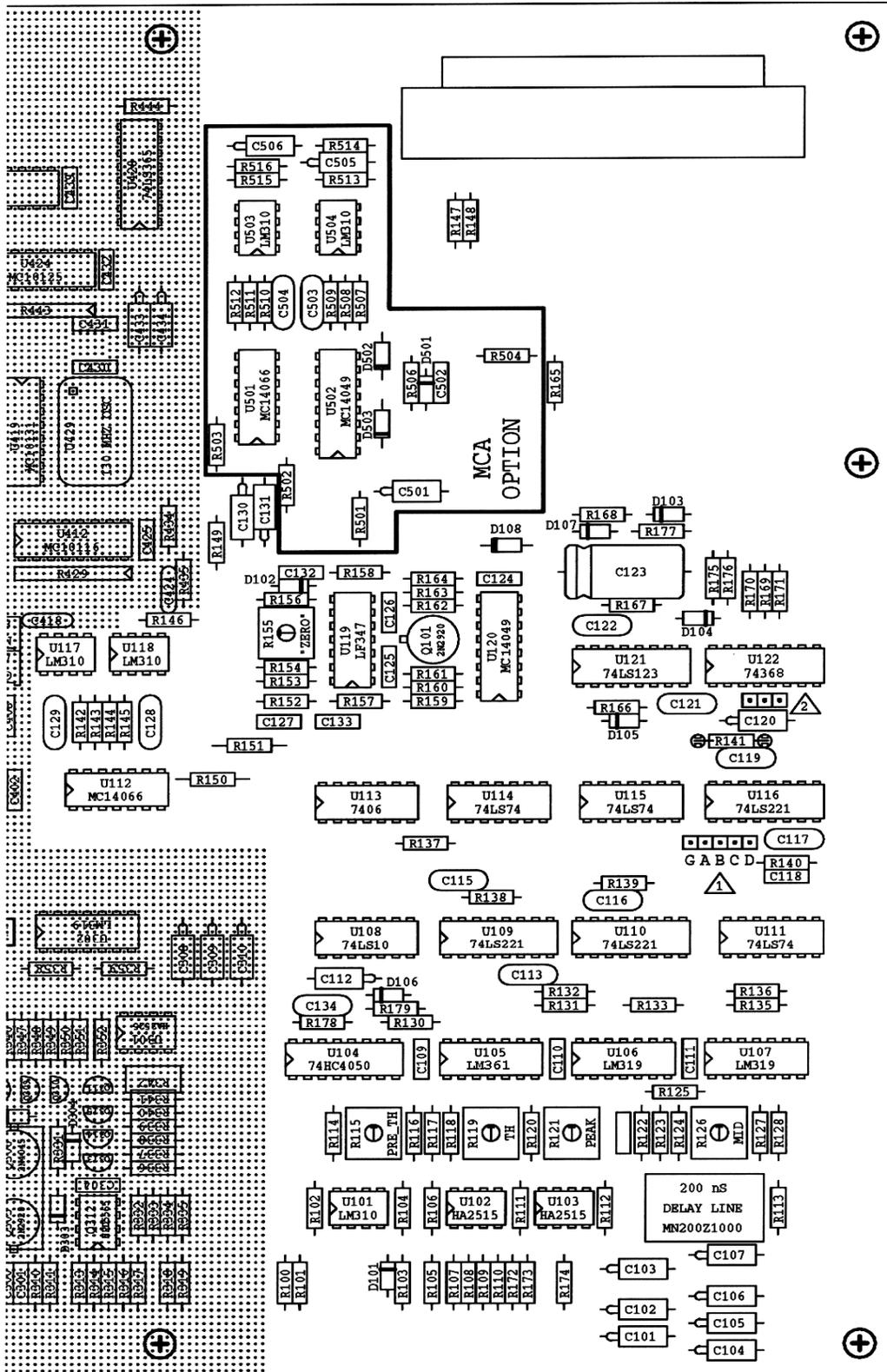
NOTES: ⚠ JUMPER SELECT FOR INTERNAL OR EXTERNAL ADC

          ⚠ JUMPER SELECT FOR ANALOG STROBE POLARITY

Figure 3-14A   X and Y Ratio Section <2,3>, Component Locator, for S/N 95467 and above
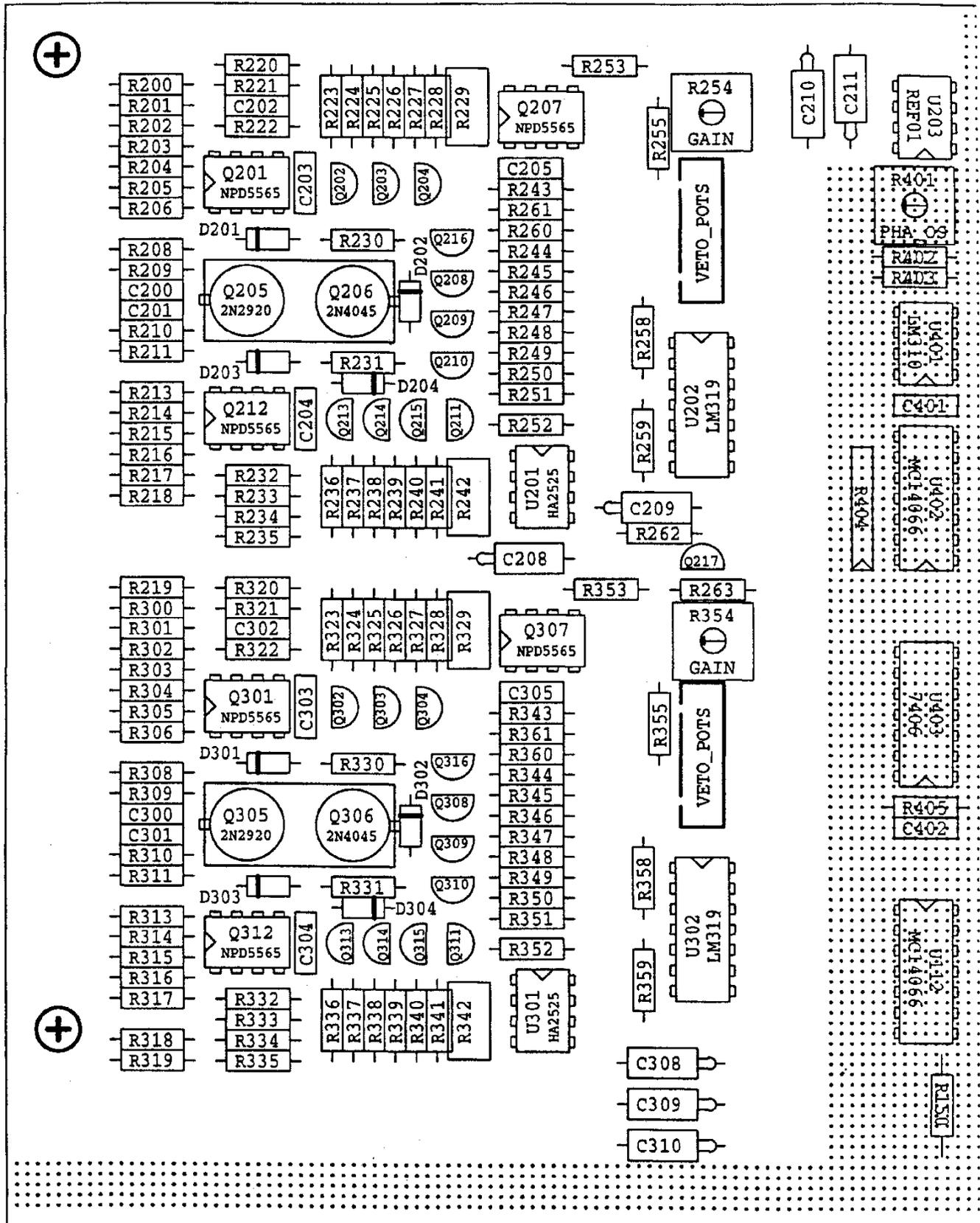
Figure 3-15A   ADC Section <4>, Component Locator, for S/N 95467 and above
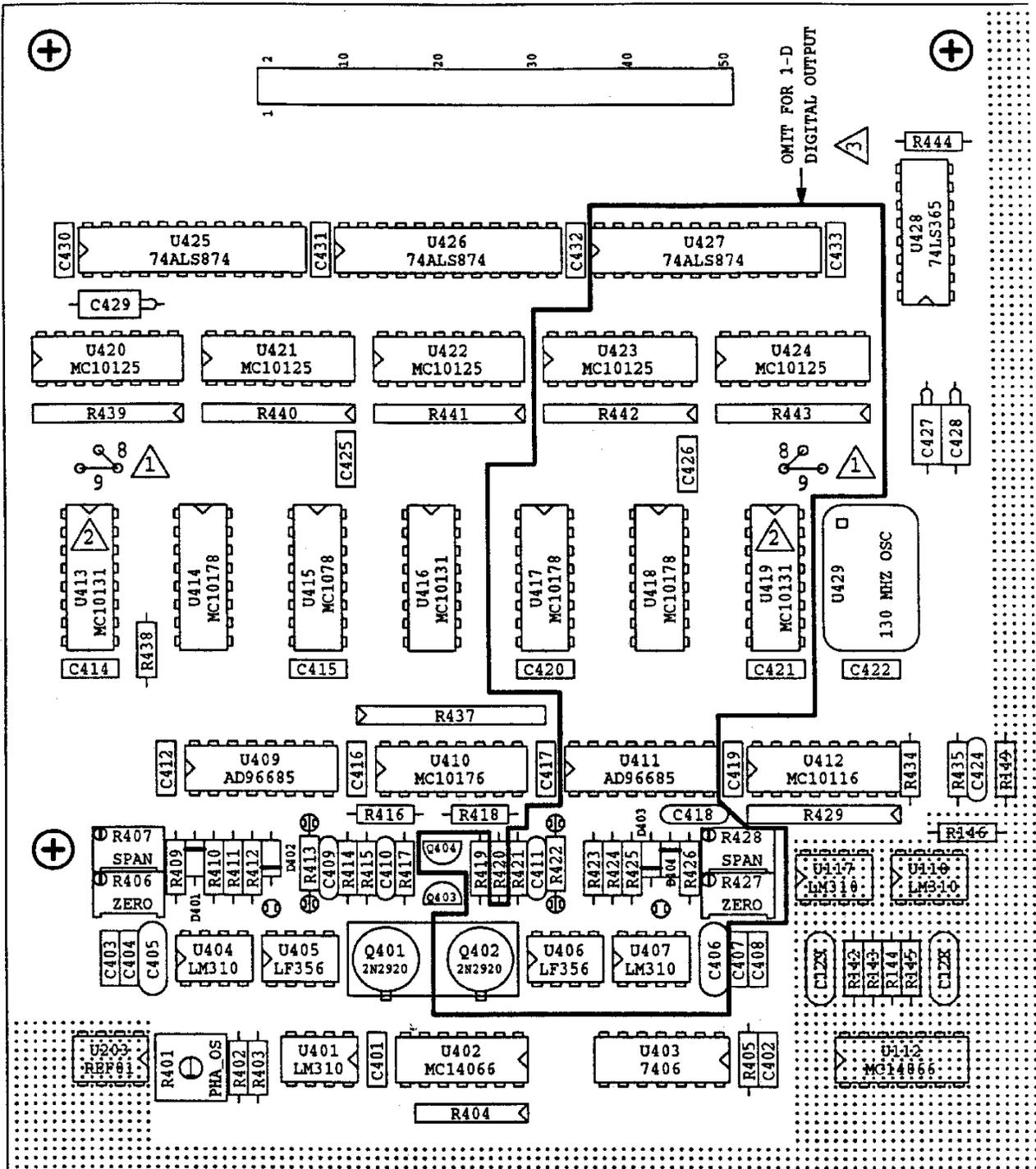
NOTES:

⚠1 JUMPER POSITIONS ARE SHOWN FOR 8 AND 9 BIT VERSIONS
     OMIT JUMPER FOR 10 BIT VERSION

⚠2 U413 AND U419 ARE OMITTED FOR 8 BIT VERSION

⚠3 X AXIS CIRCUIT IS OMITTED FOR 1D VERSION

ADC COMPONENT LOCATOR

Figure 3-16   ADC Component Values

The following values are used in the 8-bit, 9-bit and 10-bit ADC Digital Output options as shown below:

	8-bit	**9-bit**	**10-bit**
R413, R422	8.25 K	17.8 K	34.8 K
R415, R417, R419, R421	7.5 K	14.7 K	30.1 K
R132	14.7 K	20.0 K	20.0 K
SPAN pots R407 and R428	2.0 K	5.0 K	5.0 K
"ADC TIMEOUT" period (U116a) in μsec (ADC jumpers set for on-board ADC	2.4 μsec	4.4 μsec	8.4 μsec
C119	150 pF	510 pF	510 pF
Approximate Value of R141 to give correct "ADC TIMEOUT" (select for -0%, +5% limits)	22.1 K	12.1 K	24.9 K
ADC Overflow Jumper (See Note <1> on ADC Schematic	8-bit position	9-bit position	Omit

Figure 3-17   1-D/2-D Digital Memory Mapping Cable, Switch Option, Schematic and Component Locator
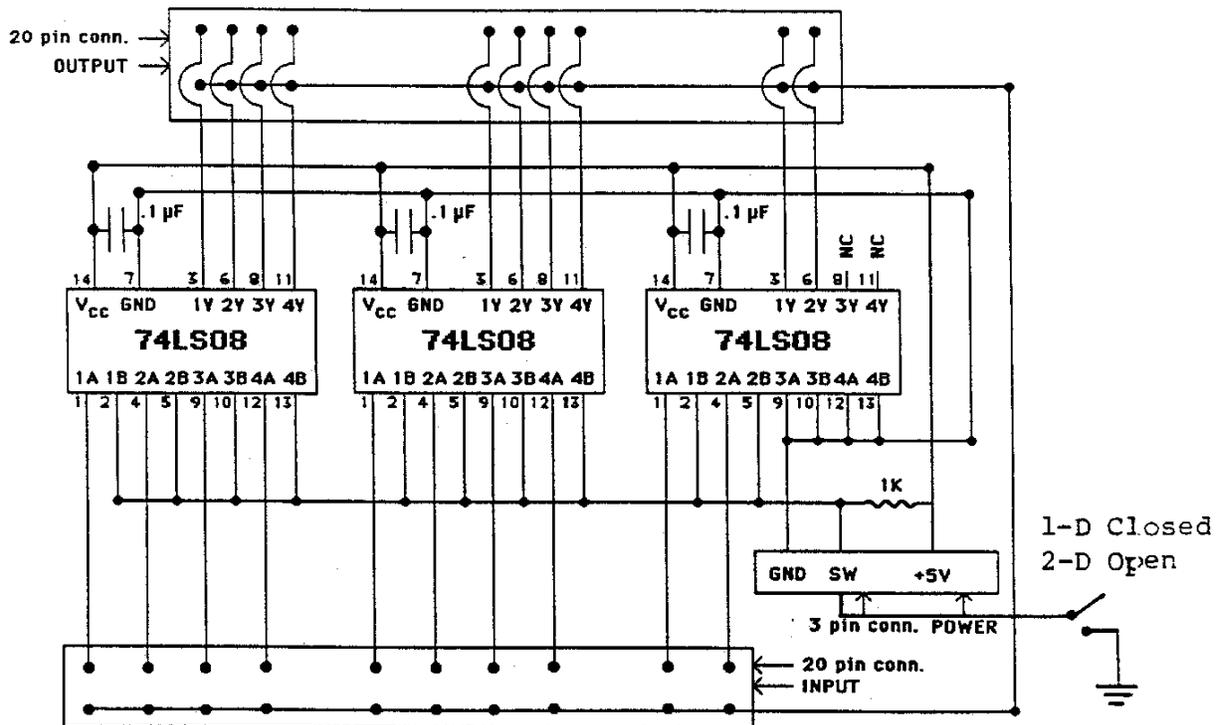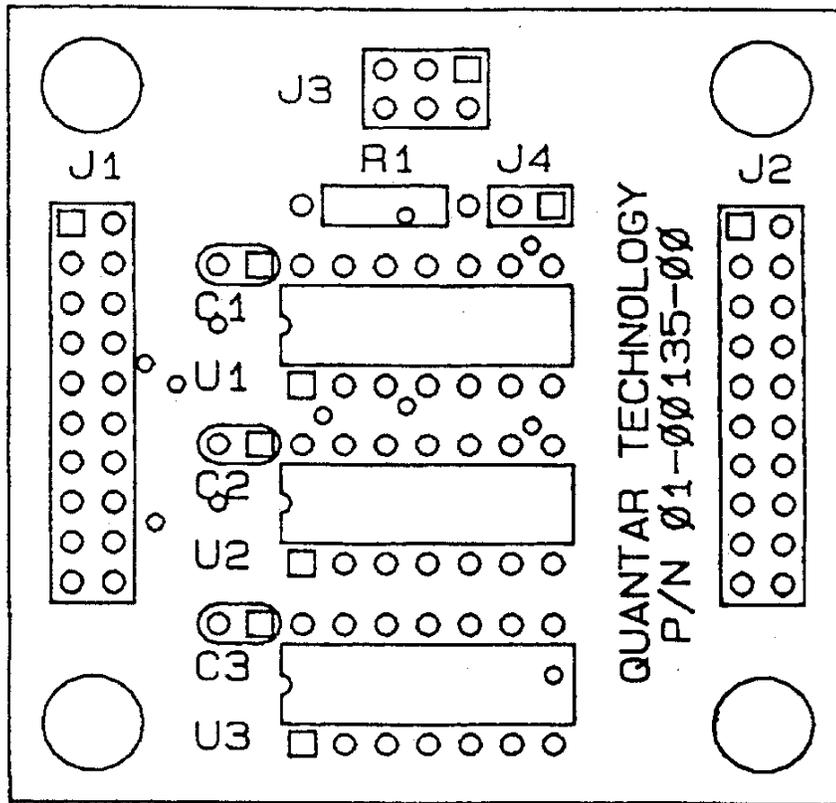
Figure 3-18A   MCA Interface, Mounted On Main Board, Schematic and Component Locator,
for S/N 7440 and above
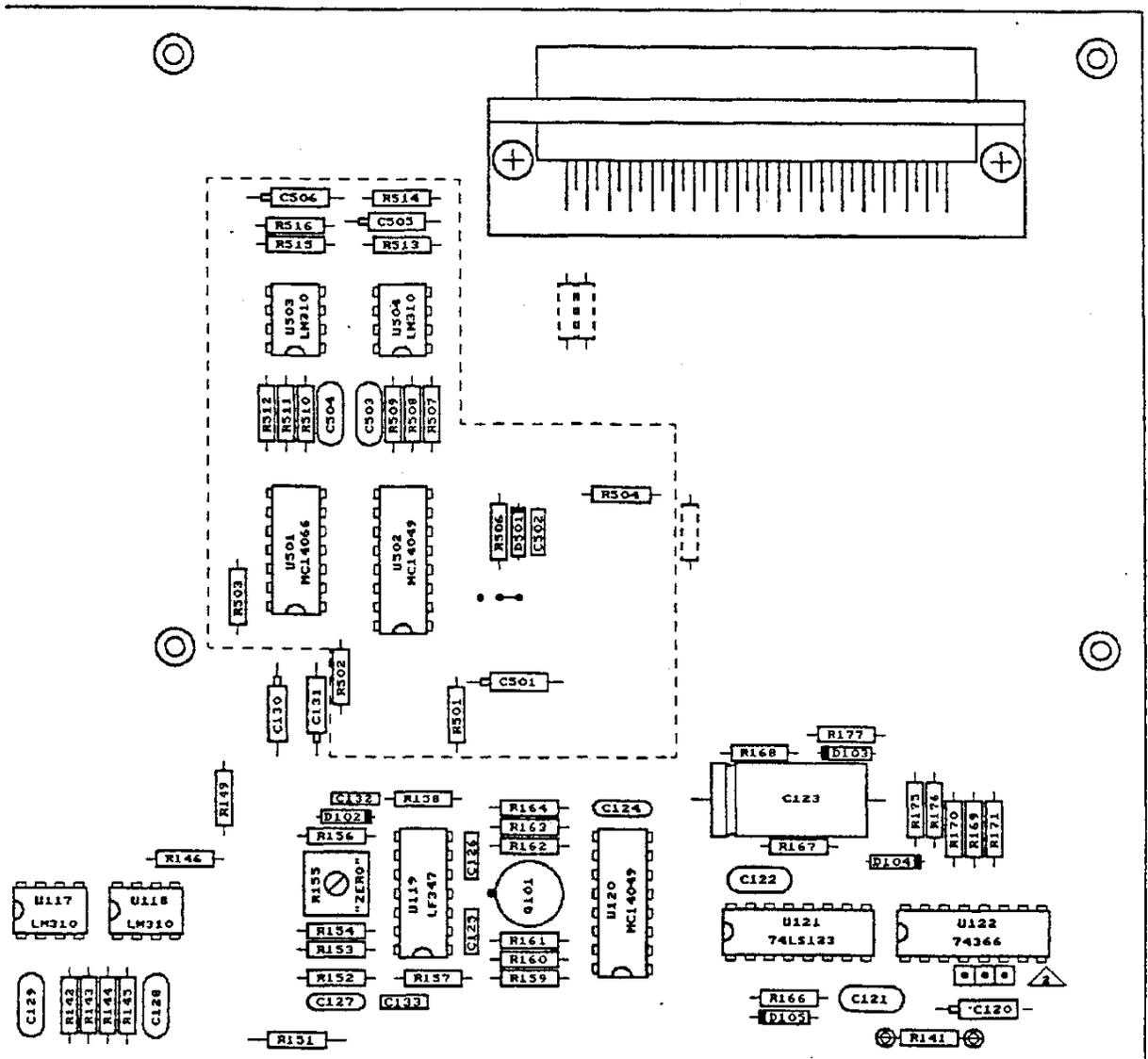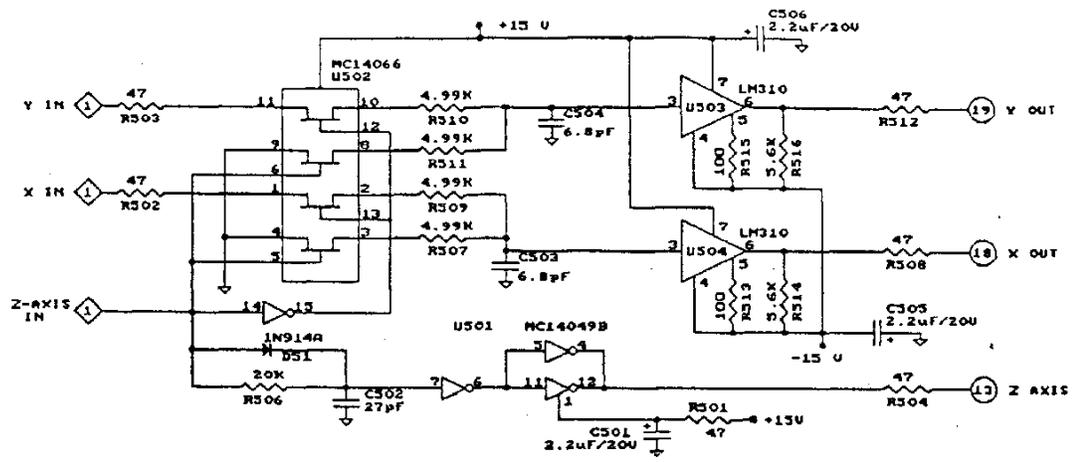
Figure 3-19A   Chassis Power Supply (dual output, modular supplies) Schematic,
for S/N 18400, 19406 and above.
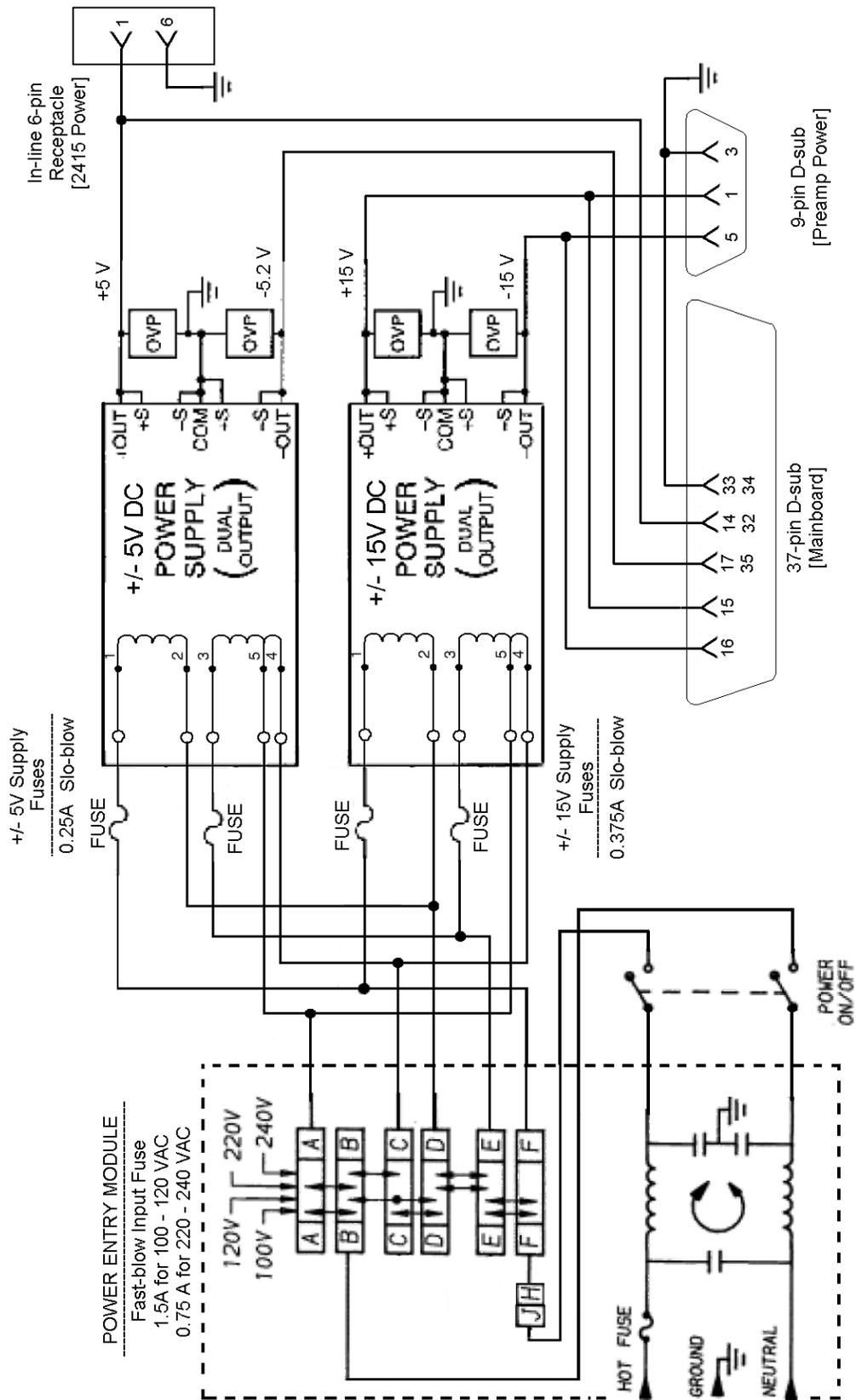
Figure 3-19B   Chassis Power Supply (dual output, modular supplies), Test Points Locator,
for S/N 18400, 19406 and above.
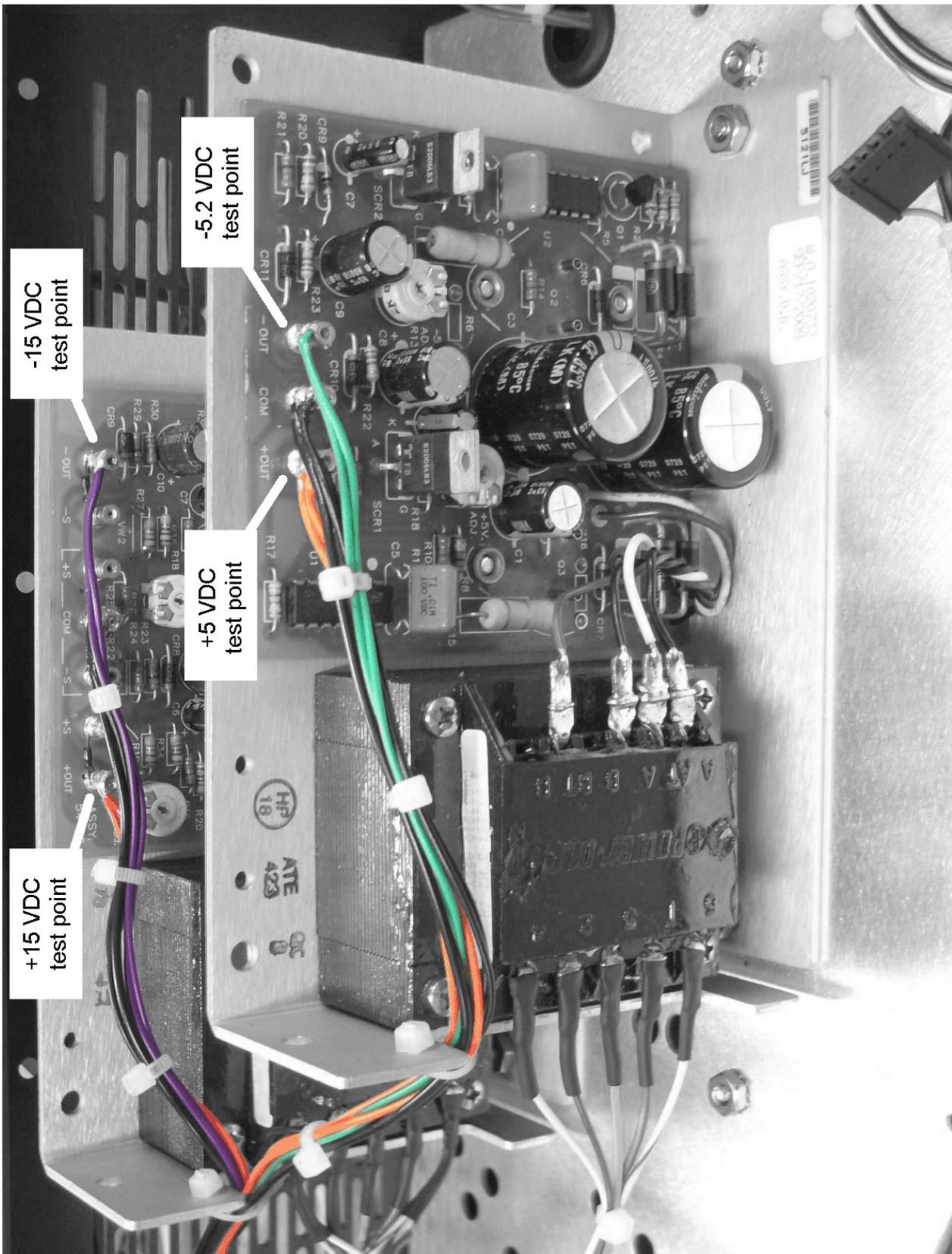
-15 VDC test point

-5.2 VDC test point
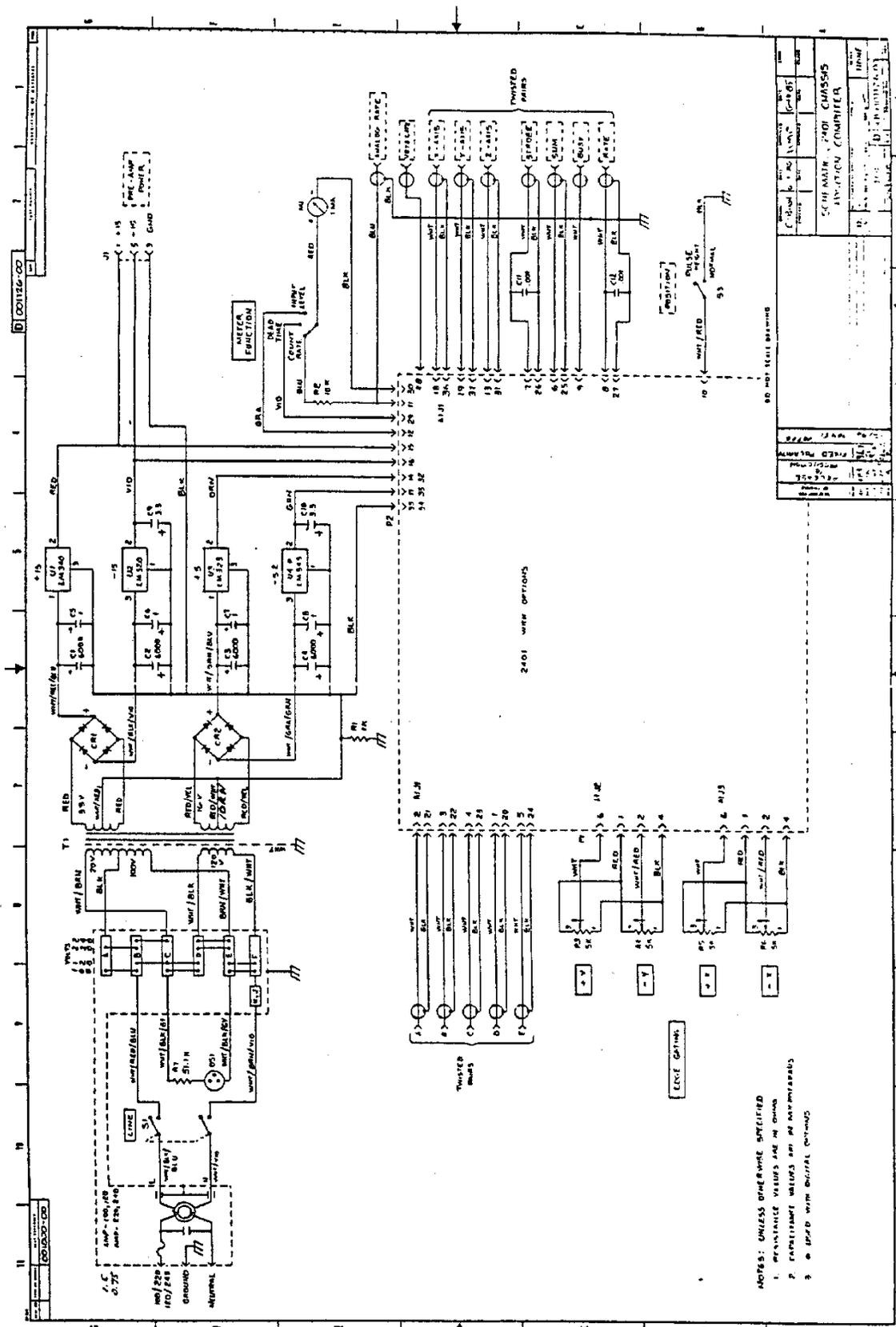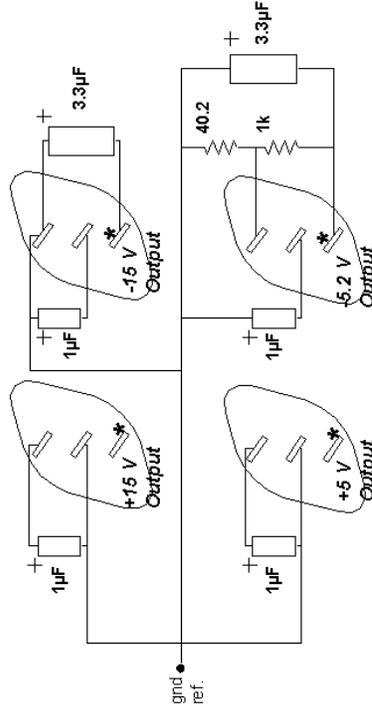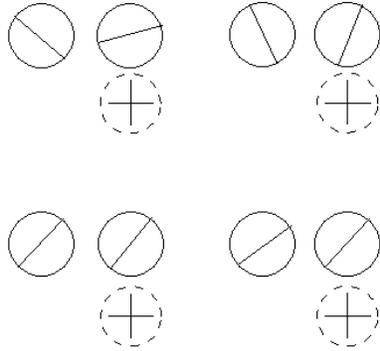
+5 VDC test point
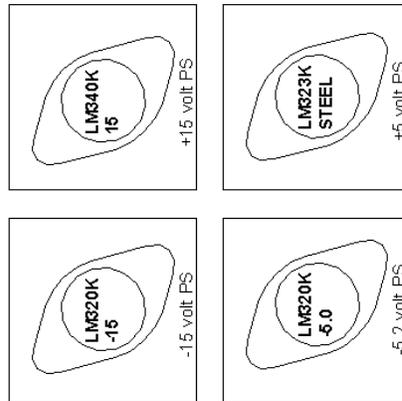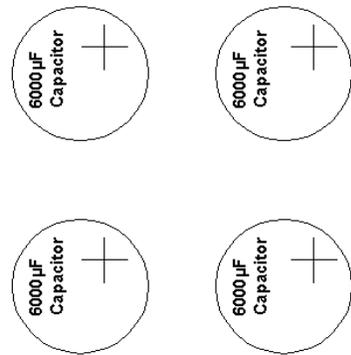
+15 VDC test point

3.3   ENGINEERING DESIGN CHANGES AND MANUAL CHANGES

The following changes were implemented in Model 2401A Position Computers and 2401B Position Analyzers with serial numbers as shown. In later units, the serial number is shown on a serial number label on the rear panel. In earlier units, the serial number is marked only on the rear edge of the main electronic board.

Manual Change Sheets update information in this Manual for later versions of the product. If such changes apply, Change Sheets are included in this section.

Serial Number 7440 and higher (approximately Jan 1988):

1.   Change made to E channel preamp termination on Control Logic section to improve pulse processing: R116 changed from 2K ohm to 22.1 ohm; R117 changed from 1K ohm to 40.2 ohm.

2.   Change to Reset Time (C113, R132) and ADC Timeout (C119, R141) to improve resolution: lengthened dead-time by approximately 0.5 seconds to present specifications. Resistor values changed to values shown in Figure 3-16, Component Values For ADC Options. U104 configuration changed.

3.   The digital output connector was changed from two 26-pin ribbon-type connectors (one for Y axis data and one for X axis data) to a single 50-pin ribbon-type connector. Correspondingly, the rear panel digital output connector configuration has been changed from two 50-pin Amphenol-type (also known as Centronics-type) connectors to a single 50-pin Amphenol-type connector, regardless of whether an optional Histogramming Buffer Memory is installed or not.

4.   Change made to charge-sensitive preamps reducing transistor current: change R8 from 10k ohm to 20k ohm, change R9 from 4.7k ohm to 10k ohm. Not critical to performance.

Serial Number 90451 and higher

1.   Model Suffix changed to Model 2401B (B version). Revised front panel. Quantar Technology name on front panel (upper left). Rectangular, rocker-type LINE power switch replaces older pushbutton switch.

2.   VETO GATE INPUT feature added and connector added to rear panel. Enables interruption of event processing by external signal. While this was provided as a special modification on earlier units, it is now standard.

3.   1-D/2-D Switch Module and rear-panel switch control of 1-D/2-D Switch Module added to enable switching between 1-D and 2-D modes for digital data collection when Histogramming Buffer Memory is installed. Previously, it was necessary to physically exchange ribbon cables when changing between 1-D to 2-D data accumulations. The 1-D/2-D Switch Module circuit board is connected in middle of Memory Mapping Cable (available for the 8-bit, 9-bit and 10-bit operation) and is powered from the Memory Power connector.

Serial Number 95467 and higher (approximately December 1995)

1.   1-D/2-D data switching function is now implemented on main circuit board rather than requiring separate 1-D/2-D Switch Module (separate PC board in cable). Can be software controlled by Model 2251A MCA/MCA2D Software versions 2.27 and later.
2.   See new Component Locator and Schematic diagrams, Figures 3-13 through 3-15. These new schematics apply to only SN 95467 and later. Contact Quantar Technology for schematics for earlier versions. +6 volt regulator has been eliminated; Analog Devices comparator now operates directly from +5 volts. Back to back diodes have been added on Z axis blanking output to partially protect against possible transient voltage from external oscilloscope Z-axis input (protects U120).

Serial Number 18400, 19406 and above (approximately September 2009 and after).

1.   Power supply change from discrete component design to dual-output linear, modular supplies.

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